

N-Channel Super Trench Power MOSFET

Description

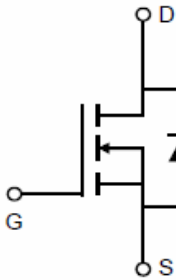
The HMS80N10DA uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS}=100V, I_D=80A$
 $R_{DS(ON)}=6.4m\Omega$ (typical) @ $V_{GS}=10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

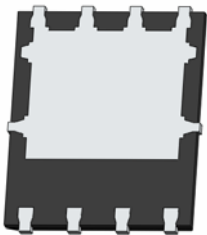
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View



Bottom View

100% UIS TESTED!
100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HMS80N10DA	HMS80N10DA	DFN5X6-8L			

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_D(100^{\circ}C)$	56	A
Pulsed Drain Current	I_{DM}	240	A
Maximum Power Dissipation	P_D	135	W
Derating factor		1.1	W/ $^{\circ}C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	676	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.93	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

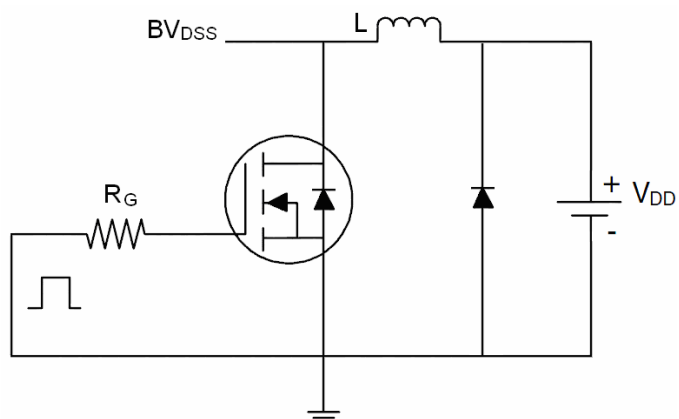
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =50A	-	6.4	7.7	mΩ
		V _{GS} =4.5V, I _D =50A	-	9.3	11.6	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =50A	40	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{ISS}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	4300	-	PF
Output Capacitance	C _{OSS}		-	790	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	47	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =50A V _{GS} =10V, R _G =4.7Ω	-	13	-	nS
Turn-on Rise Time	t _r		-	58	-	nS
Turn-Off Delay Time	t _{d(off)}		-	39	-	nS
Turn-Off Fall Time	t _f		-	8	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =50A, V _{GS} =10V	-	60		nC
Gate-Source Charge	Q _{gs}		-	21		nC
Gate-Drain Charge	Q _{gd}		-	11		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =50A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	80	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs (Note3)	-	60		nS
Reverse Recovery Charge	Q _{rr}		-	140		nC

Notes:

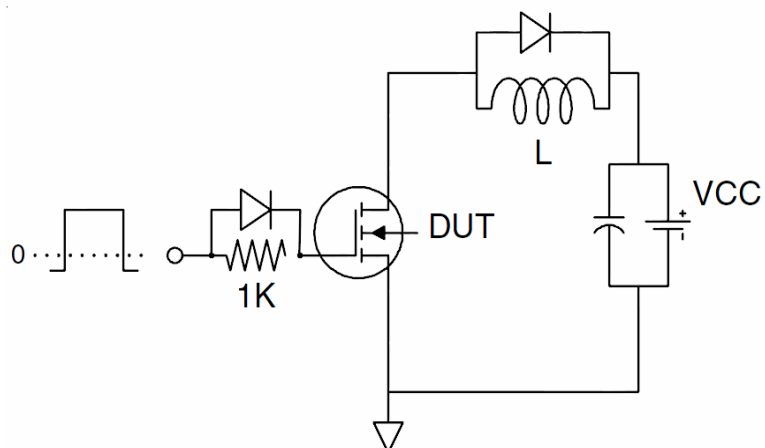
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

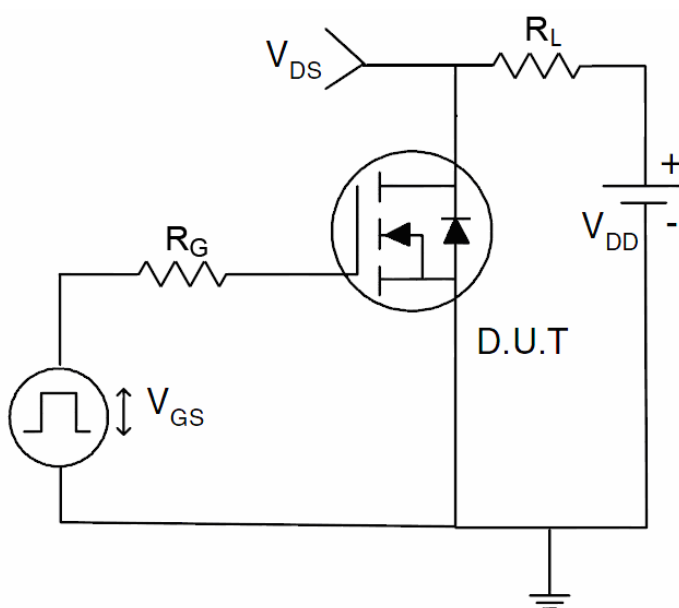
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

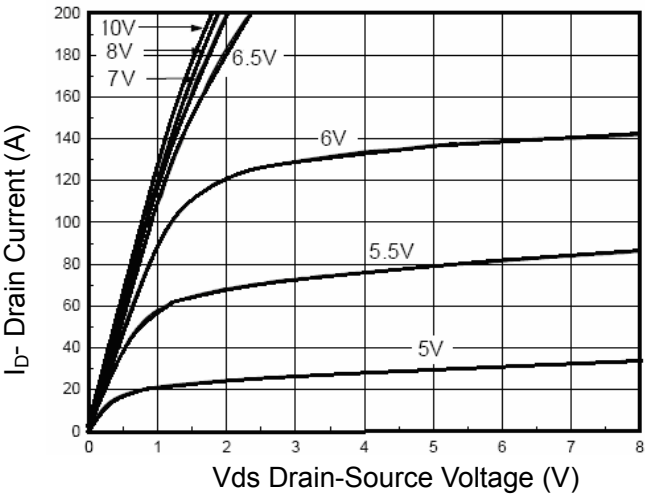


Figure 1 Output Characteristics

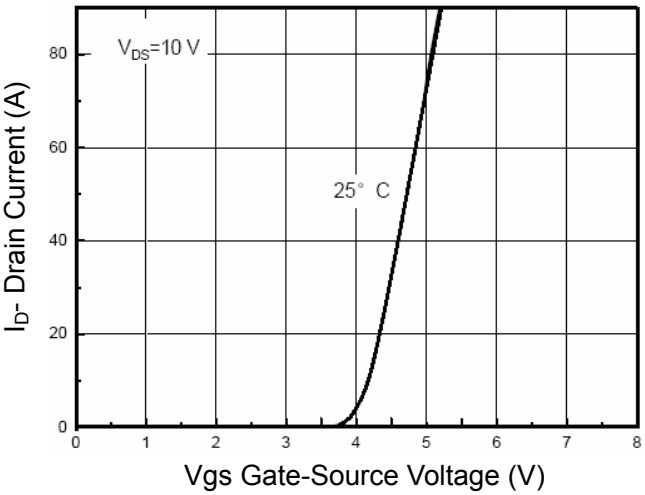


Figure 2 Transfer Characteristics

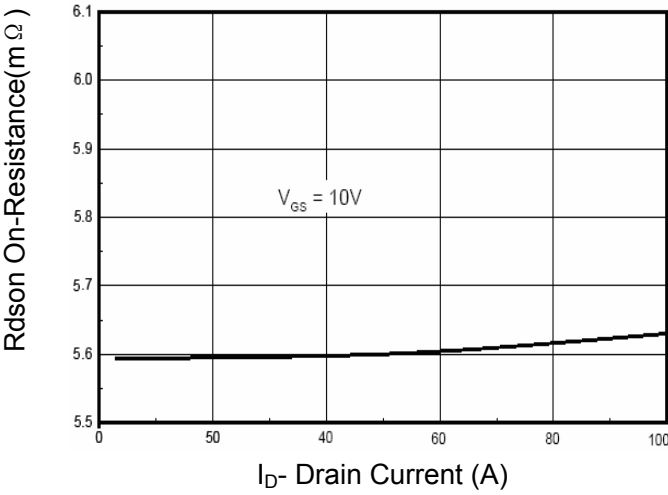


Figure 3 $R_{DS(on)}$ - Drain Current

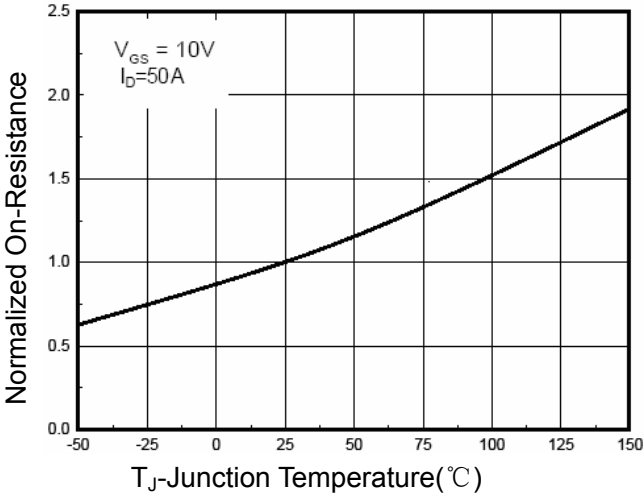


Figure 4 $R_{DS(on)}$ -Junction Temperature

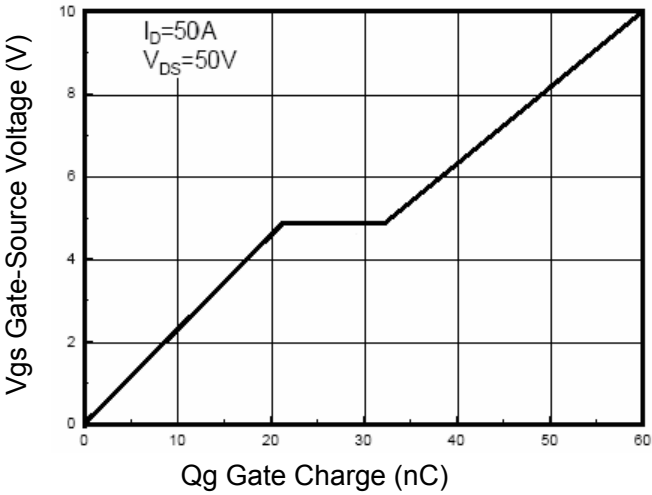


Figure 5 Gate Charge

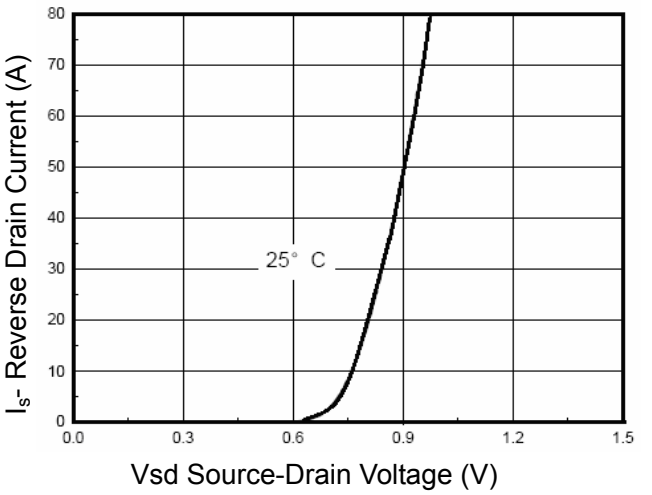


Figure 6 Source- Drain Diode Forward

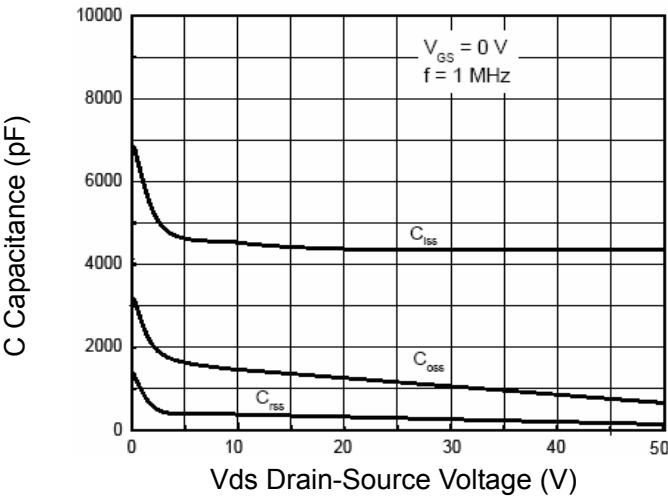


Figure 7 Capacitance vs Vds

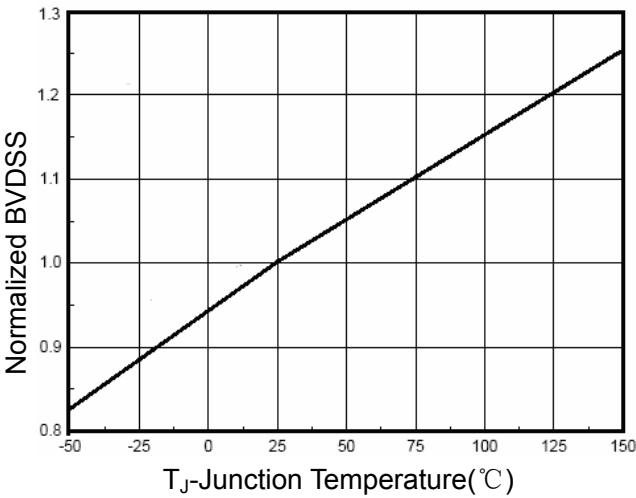


Figure 9 BV_{DSS} vs Junction Temperature

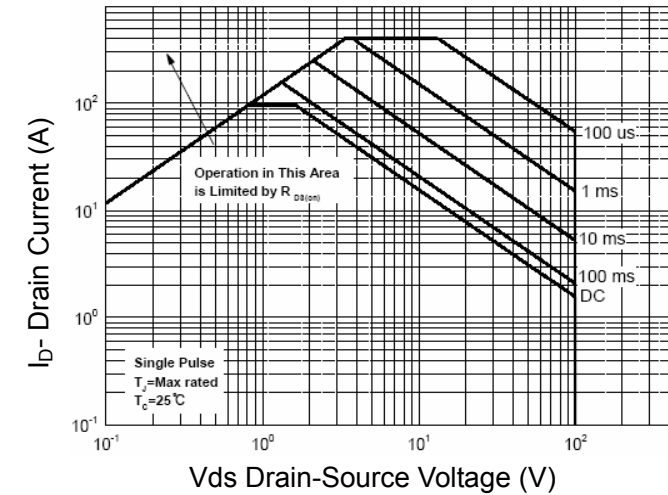


Figure 8 Safe Operation Area

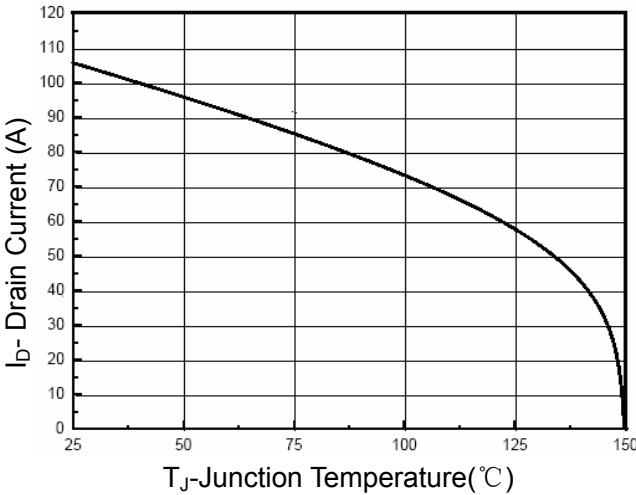


Figure 10 Current De-rating

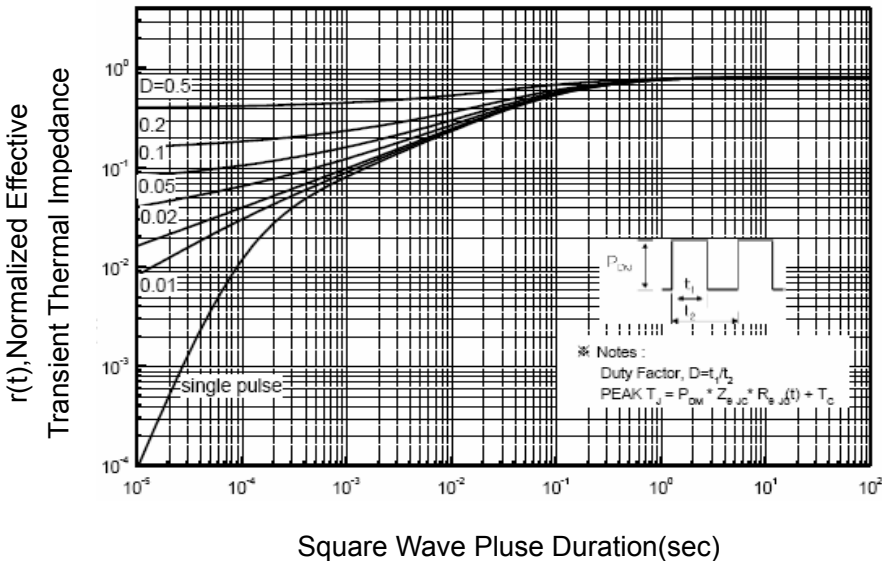
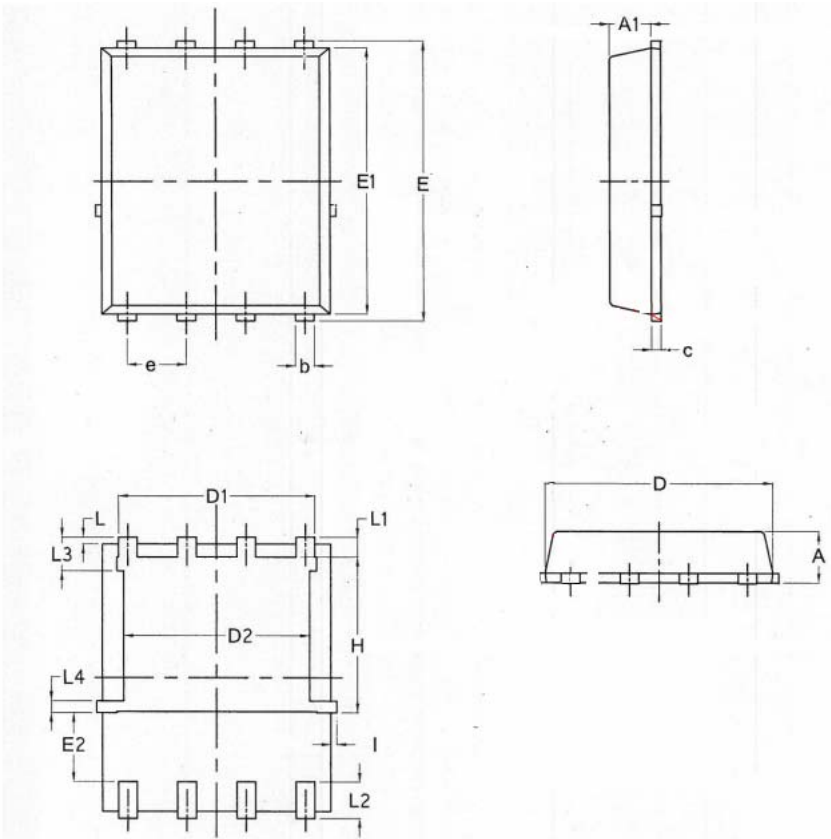


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.90	1.10	1.17	0.0354	0.0433	0.0461
A1	0.824	0.897	0.97	0.0324	0.0353	0.0382
b	0.33	0.41	0.50	0.0130	0.0161	0.0197
C	0.150	0.20	0.250	0.0059	0.0079	0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
D1	3.91	4.22	4.36	0.1539	0.1661	0.1717
D2	3.85	4.00	4.15	0.1516	0.1575	0.1634
E	5.90	60.5	6.15	0.2323	0.2382	0.2421
E1	5.65	5.76	5.85	0.2224	0.2268	0.2303
E2	1.10	/	/	0.0433	/	/
e	1.27 BSC			0.050 BSC		
L	0.05	0.15	0.25	0.0020	0.0059	0.0098
L1	0.38	0.425	0.50	0.0150	0.0167	0.0197
L2	0.51	0.785	0.86	0.0201	0.0309	0.0339
L3	0.55	0.70	0.85	0.0217	0.0276	0.0335
L4	0.10	0.25	0.40	0.0039	0.0098	0.0157
H	3.25	3.35	3.58	0.1280	0.1319	0.1409
I	0	/	0.18	0	/	0.0071