HM7N65K / HM7N65I

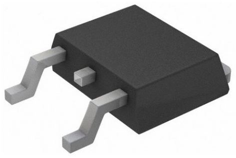
650V N-Channel MOSFET

General Description

This Power MOSFET is produced using SL semi‘s advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 7.0A, 650V, $R_{DS(on)}$ = 1.35Ω @V_{GS} = 10 V
- Low gate charge (typical 29nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



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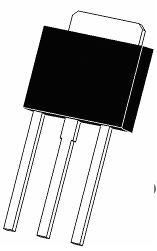

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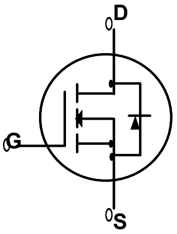


Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		HM7N65K	HM7N65I	Units
V_{DSS}	Drain-Source Voltage		650		V
I_D	Drain Current - Continuous (T_C = 25°C)		7.0	7.0*	A
	- Continuous (T_C = 100°C)		4.2	4.2 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	28	28 *	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	230		mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	14.7		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25°C)		147	48	W
	- Derate above 25°C		1.18	0.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	HM7N65K	HM7N65I	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.85	2.6	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	650	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 520 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A	--	1.1	1.35	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1000	--	pF
C_{oss}	Output Capacitance		--	110	--	pF
C_{rss}	Reverse Transfer Capacitance		--	12.6	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325 V, I_D = 7.0A, R_G = 25 Ω (Note 4, 5)	--	20	--	ns
t_r	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	80	--	ns
t_f	Turn-Off Fall Time		--	70	--	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 7.0 A, V_{GS} = 10 V (Note 4, 5)	--	29	-	nC
Q_{gs}	Gate-Source Charge		--	4.7	--	nC
Q_{gd}	Gate-Drain Charge		--	12.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	28.0	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.5 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7.5 A, dI_F / dt = 100 A/μs (Note 4)	--	350	--	ns
Q_{rr}	Reverse Recovery Charge		--	3.3	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 7.3 mH, I_{AS} = 7.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 7.0 A, di/dt ≤ 200A/μs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

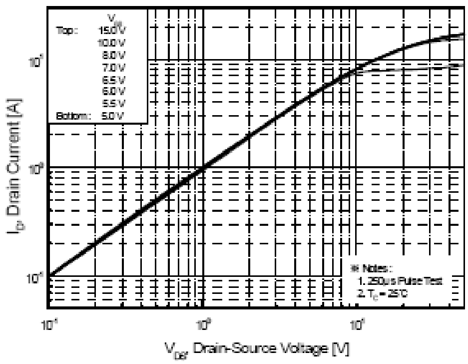


Figure 1. On-Region Characteristics

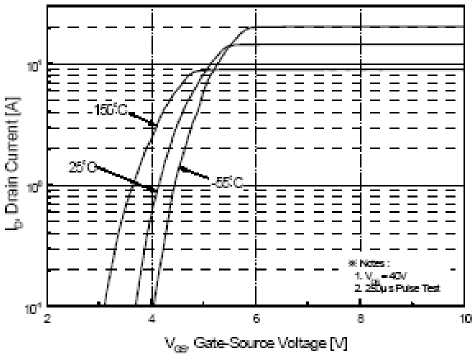


Figure 2. Transfer Characteristics

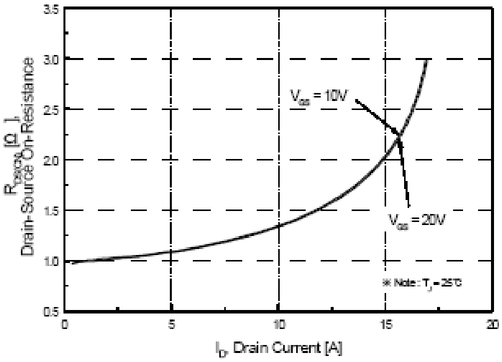


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

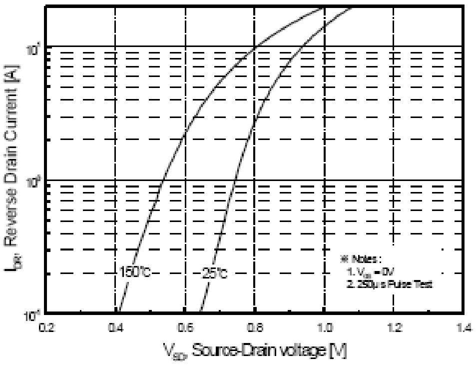


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

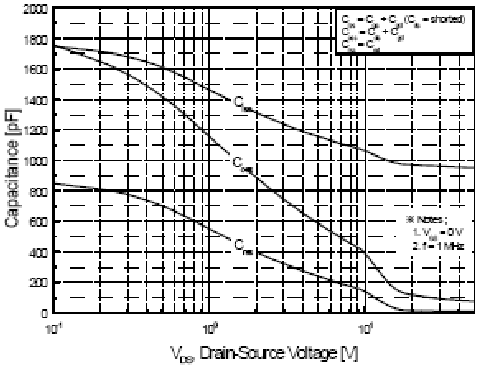


Figure 5. Capacitance Characteristics

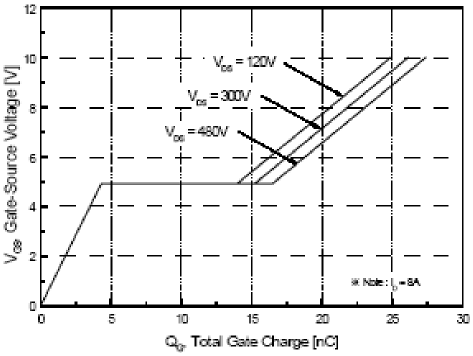


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

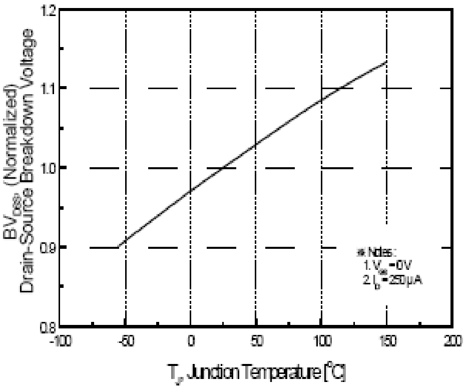


Figure 7. Breakdown Voltage Variation vs Temperature

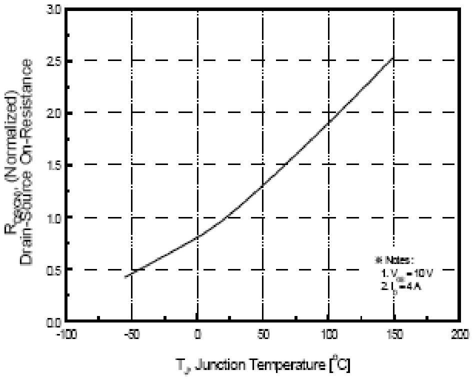


Figure 8. On-Resistance Variation vs Temperature

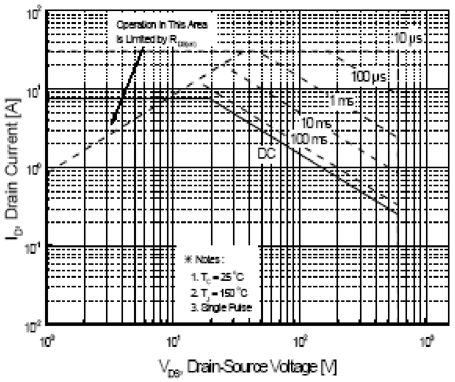


Figure 9-1. Maximum Safe Operating Area for HM7N65K

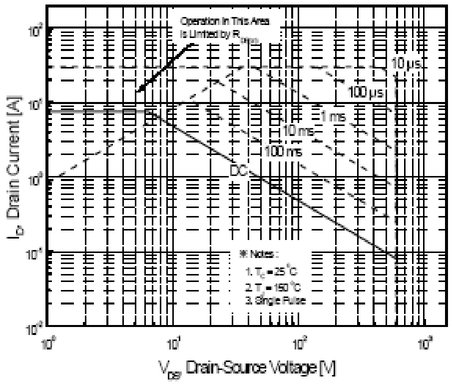


Figure 9-2. Maximum Safe Operating Area for HM7N65I

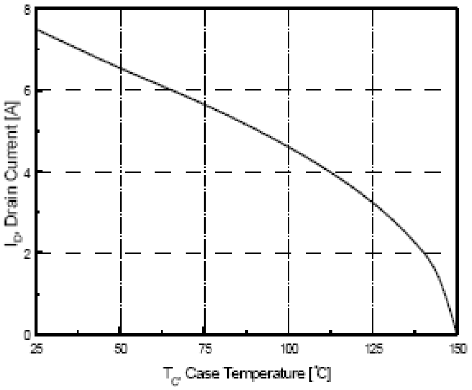


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

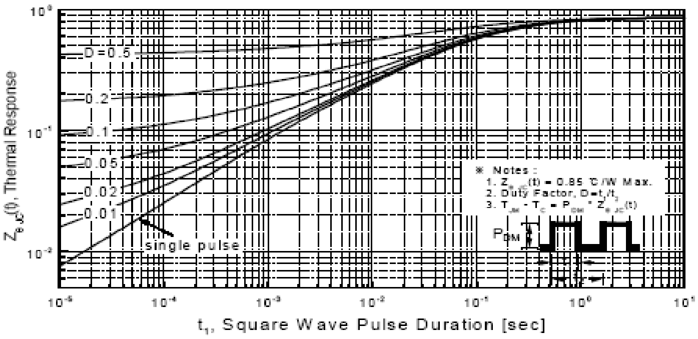


Figure 11-1. Transient Thermal Response Curve
for HM7N65K

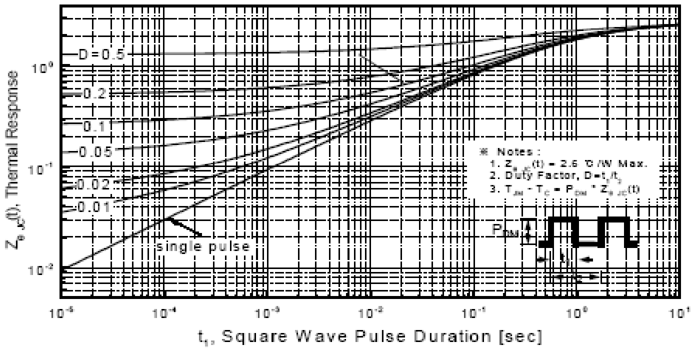
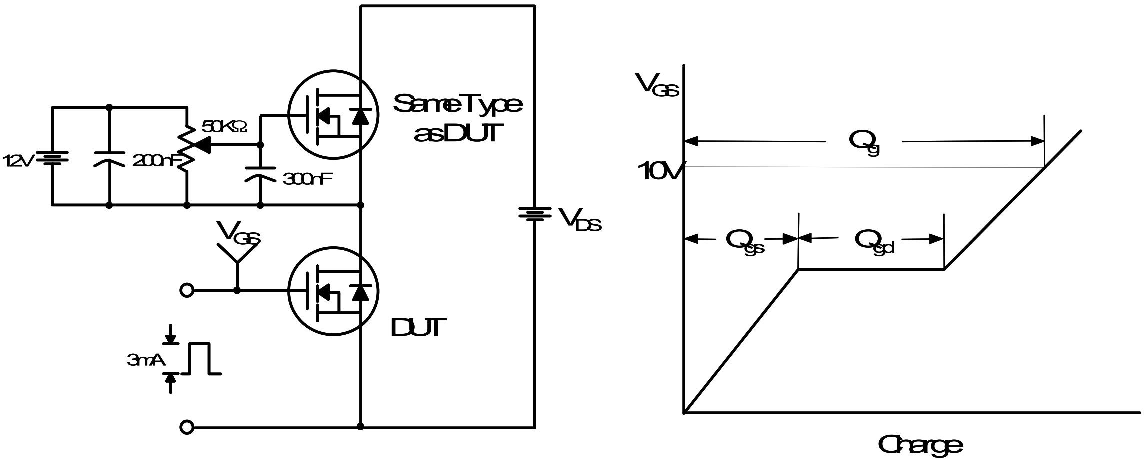
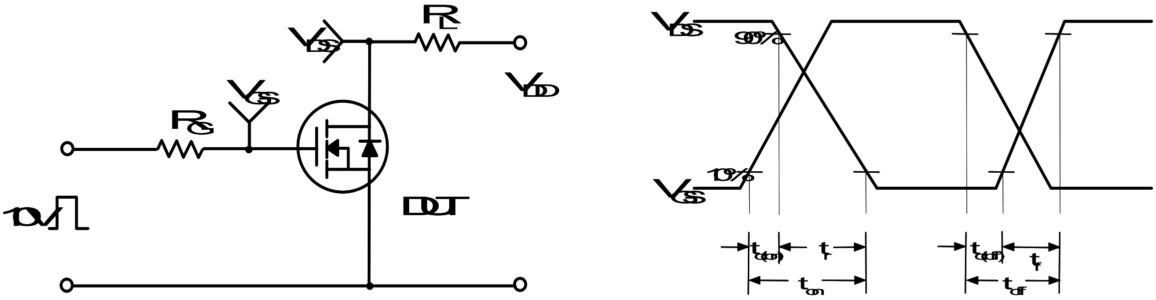


Figure 11-2. Transient Thermal Response Curve
for HM7N65I

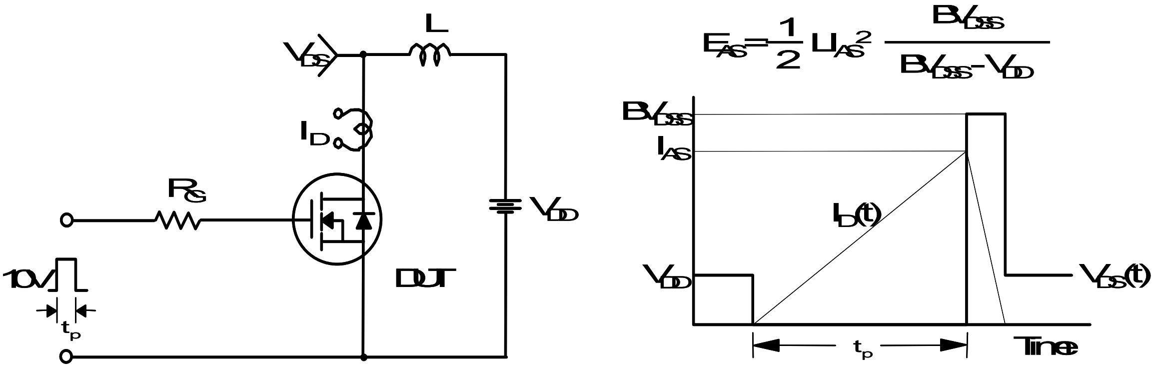
Gate Charge Test Circuit & Waveform



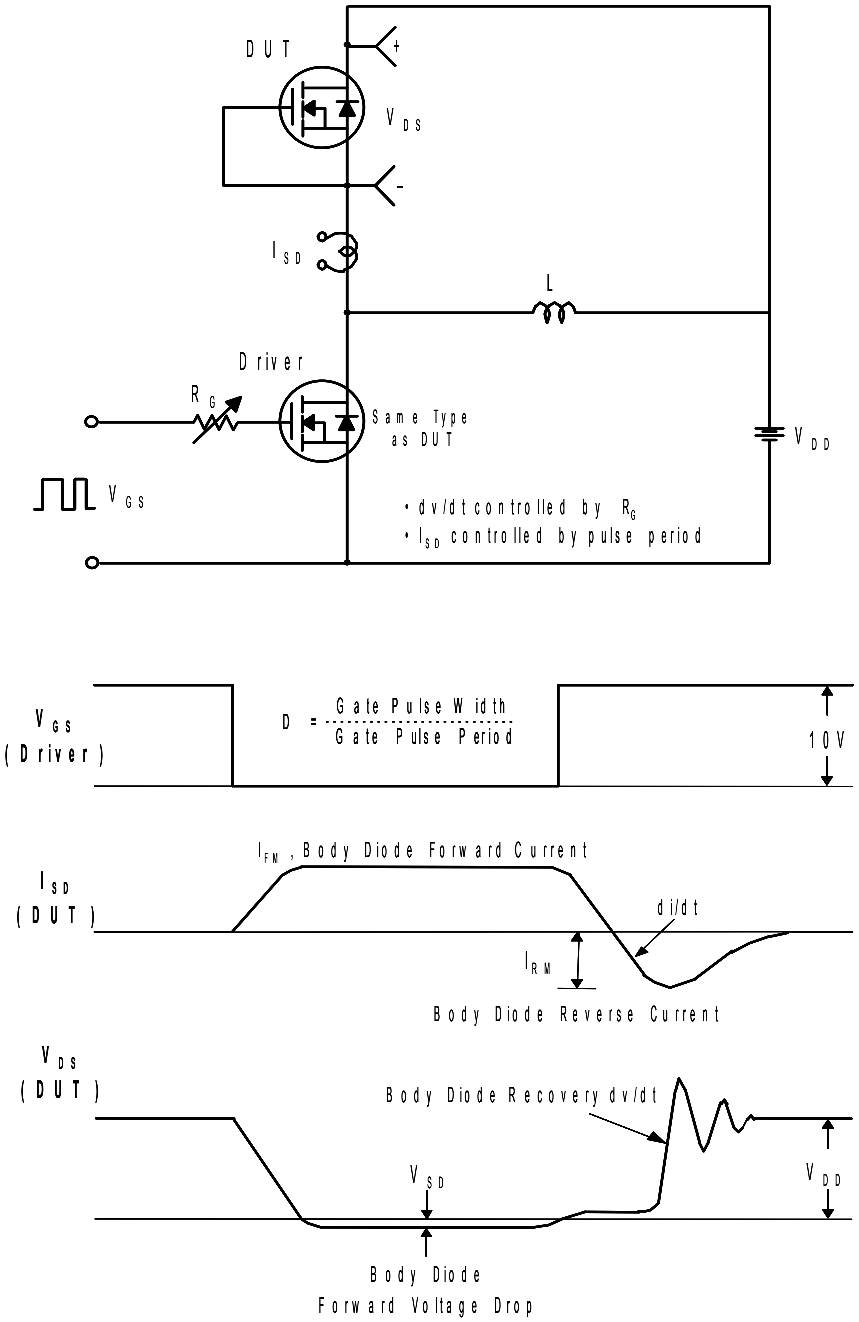
Resistive Switching Test Circuit & Waveforms



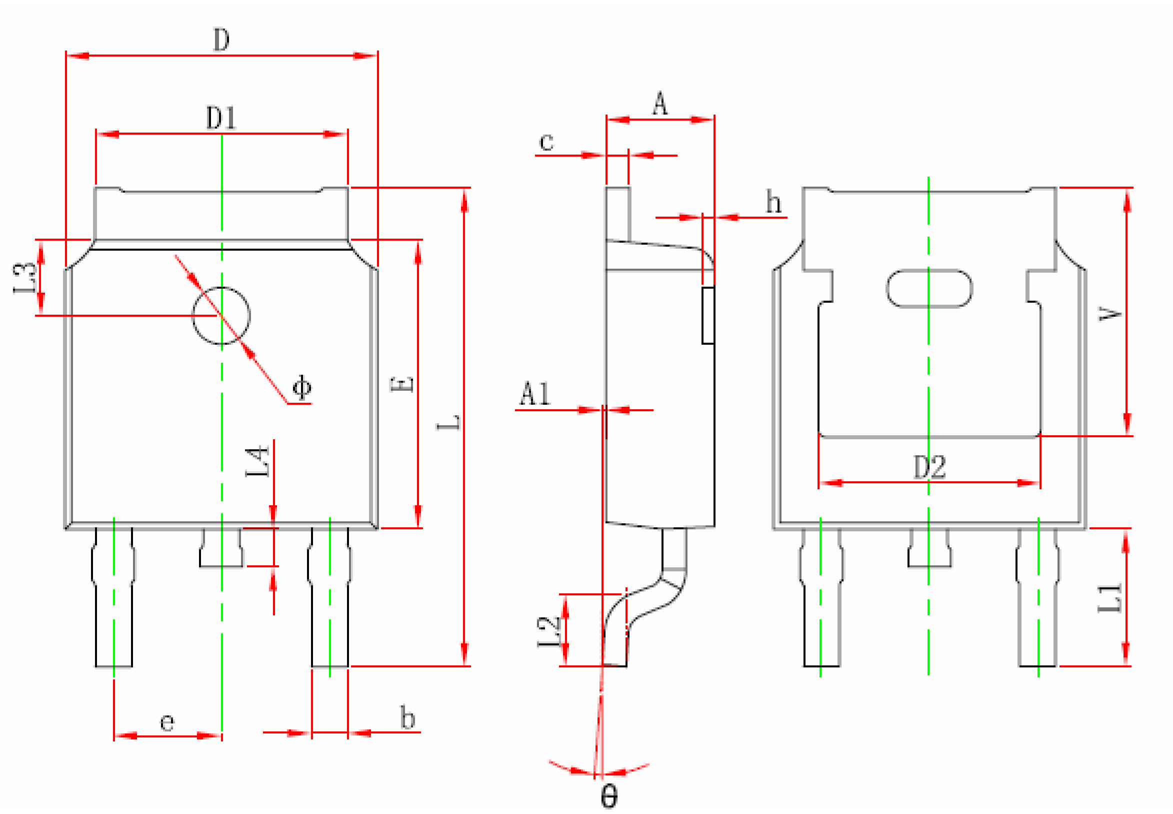
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	