

P-Channel Enhancement Mode Power MOSFET

Description

The HM35P04D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.

General Features

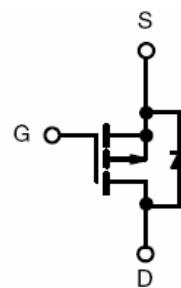
- $V_{DS} = -40V, I_D = -35A$
- $R_{DS(ON)} < 10m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

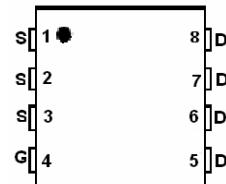
- Power switch
- Load switch in high current applications
- DC/DC converters

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM35P04D	HM35P04D	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-35	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D (100^\circ C)$	-25	A
Pulsed Drain Current	I_{DM}	-105	A
Maximum Power Dissipation	P_D	65	W
Derating factor		0.52	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	1020	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	R _{θJC}	1.92	°C/W
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Electrical Characteristics (T_c=25°C unless otherwise noted)

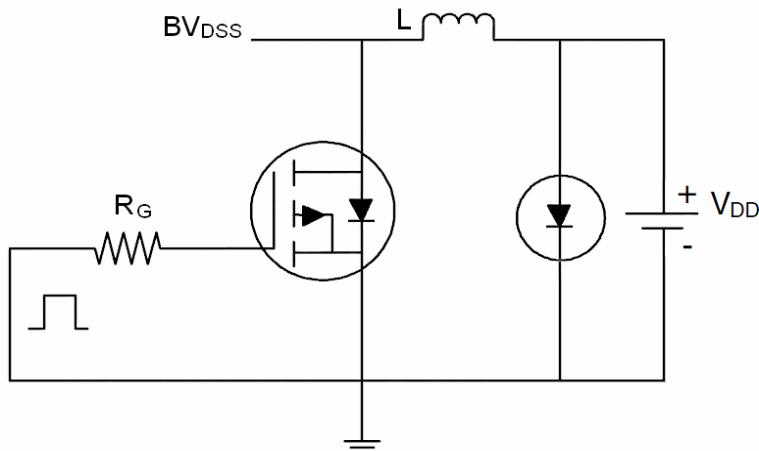
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	V _{DSS}	V _{GS} =0V I _D =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A	-	7.5	10	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-20A	-	50	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, F=1.0MHz	-	6460	-	PF
Output Capacitance	C _{oss}		-	684	-	PF
Reverse Transfer Capacitance	C _{rss}		-	600	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V, R _L =2Ω, V _{GS} =-10V, R _G =1Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	35	-	nS
Turn-Off Fall Time	t _f		-	18	-	nS
Total Gate Charge	Q _g	V _{DS} =-20, I _D =-20A, V _{GS} =-10V	-	106	-	nC
Gate-Source Charge	Q _{gs}		-	22	-	nC
Gate-Drain Charge	Q _{gd}		-	27	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-10A	-		-1.2	V
Diode Forward Current (Note 2)	I _S		-	-	-35	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, IF = - 10A di/dt = -100A/μs(Note3)	-	53	-	nS
Reverse Recovery Charge	Q _{rr}		-	50	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

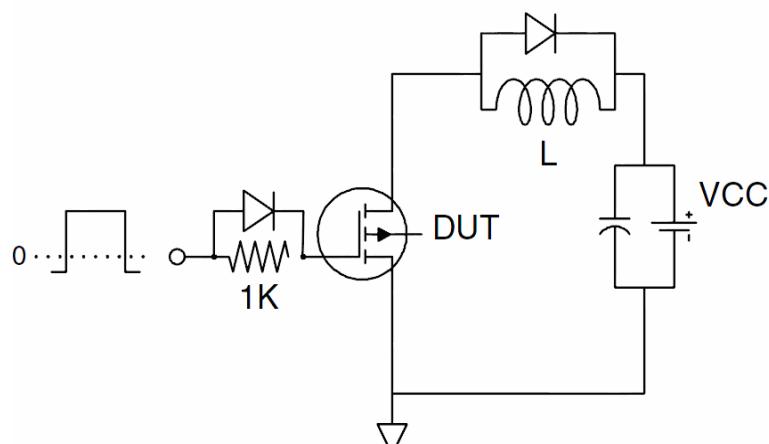
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: T_j=25°C, V_{DD}=-20V, V_G=-10V, L=1mH, R_g=25Ω, I_{AS}=45A

Test Circuit

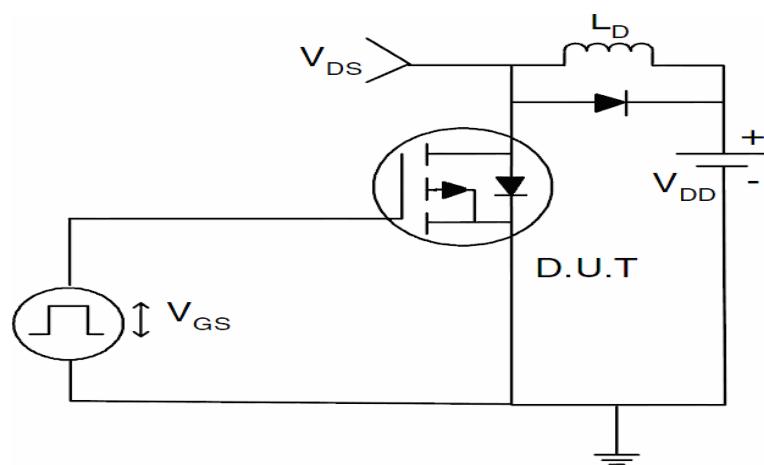
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

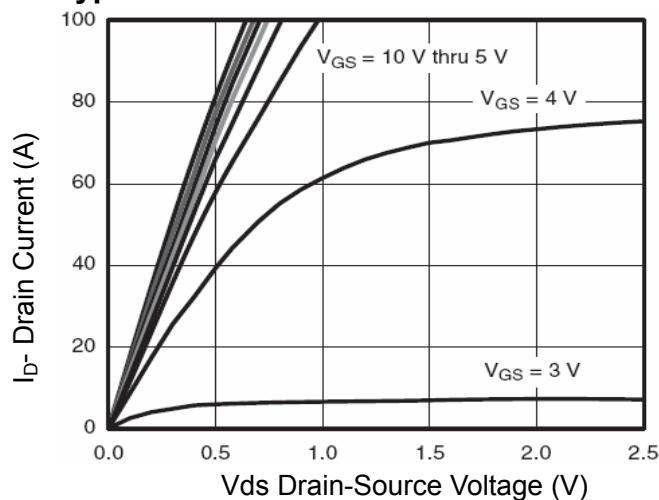


Figure 1 Output Characteristics

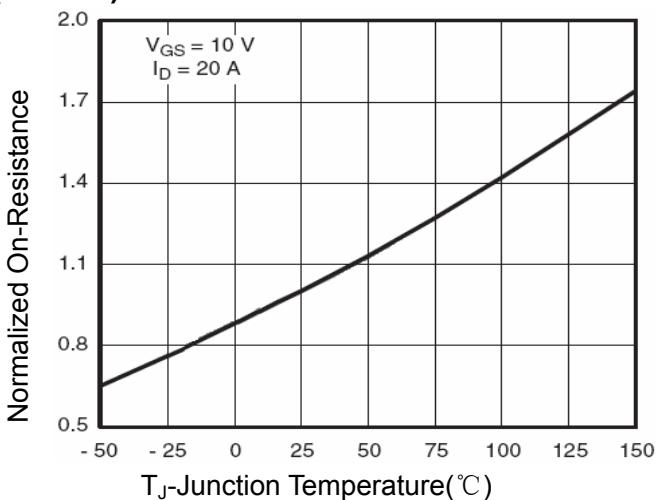


Figure 4 $R_{DS(on)}$ -Junction Temperature

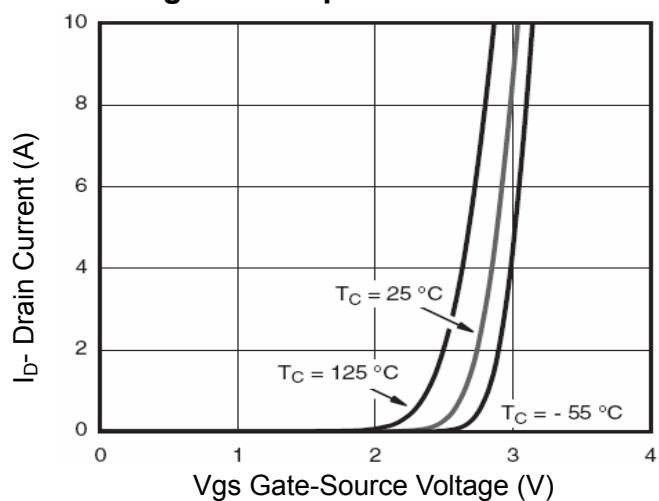


Figure 2 Transfer Characteristics

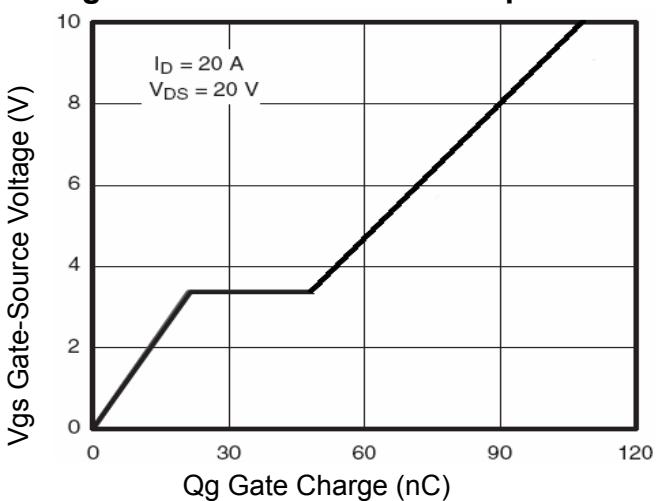


Figure 5 Gate Charge

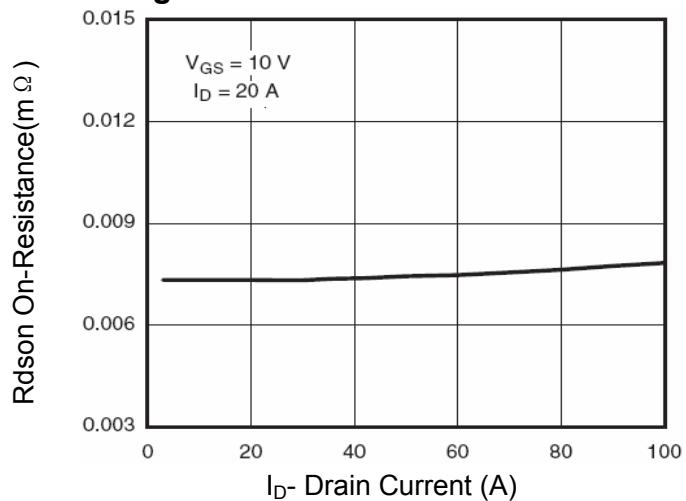


Figure 3 $R_{DS(on)}$ - Drain Current

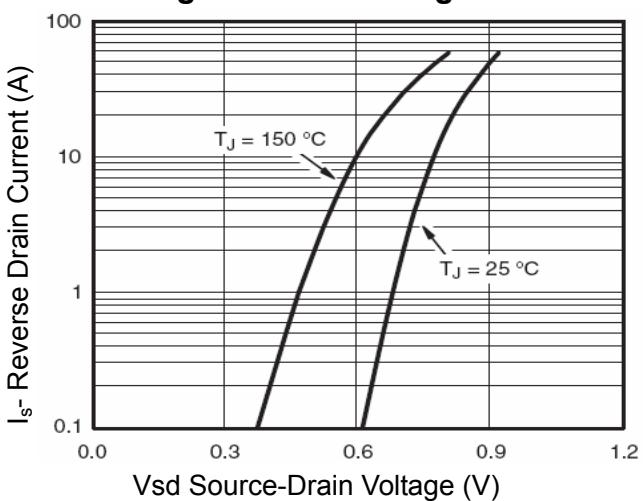


Figure 6 Source-Drain Diode Forward

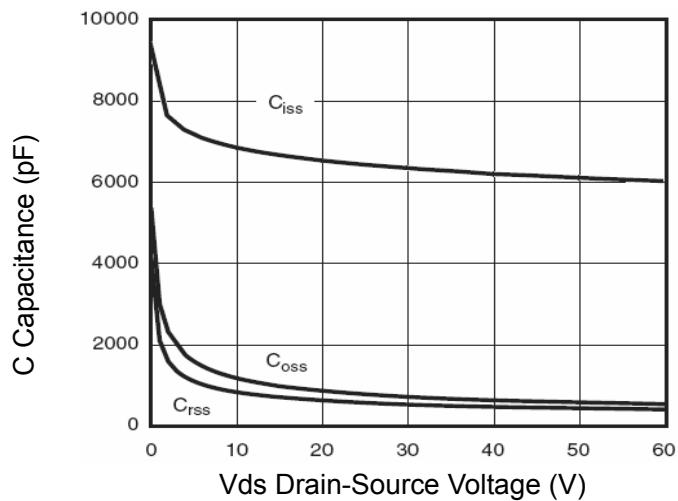


Figure 7 Capacitance vs Vds

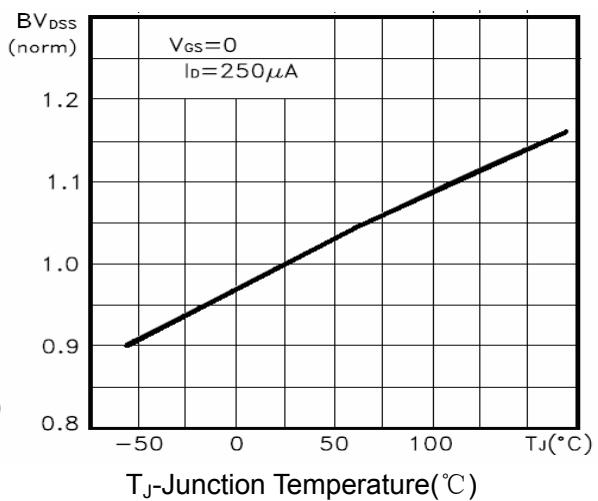


Figure 9 BV_{DSS} vs Junction Temperature

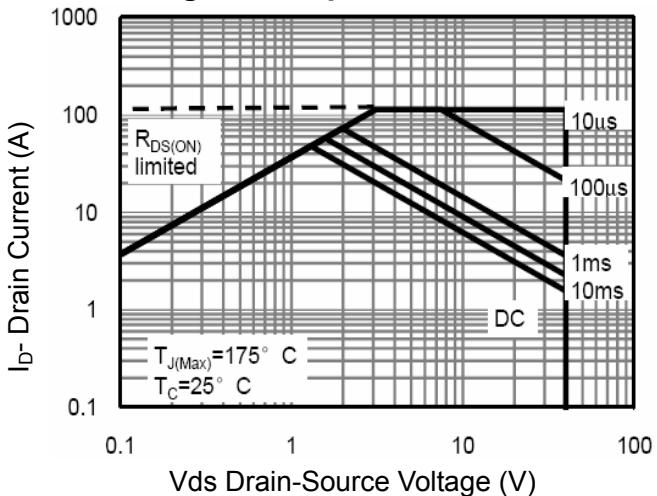


Figure 8 Safe Operation Area

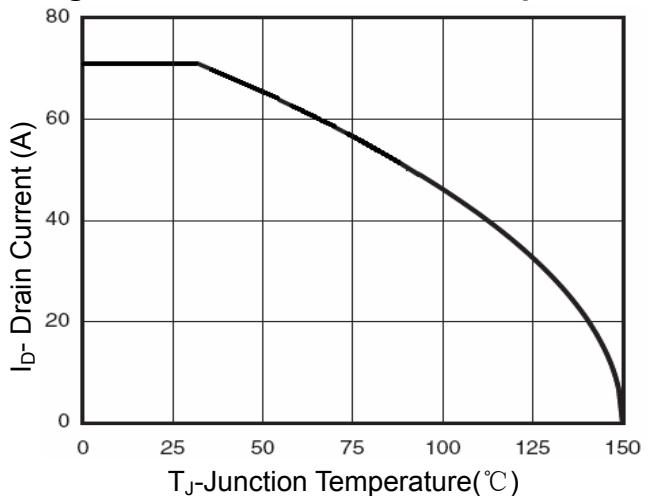


Figure 10 ID Current Derating vs Junction Temperature

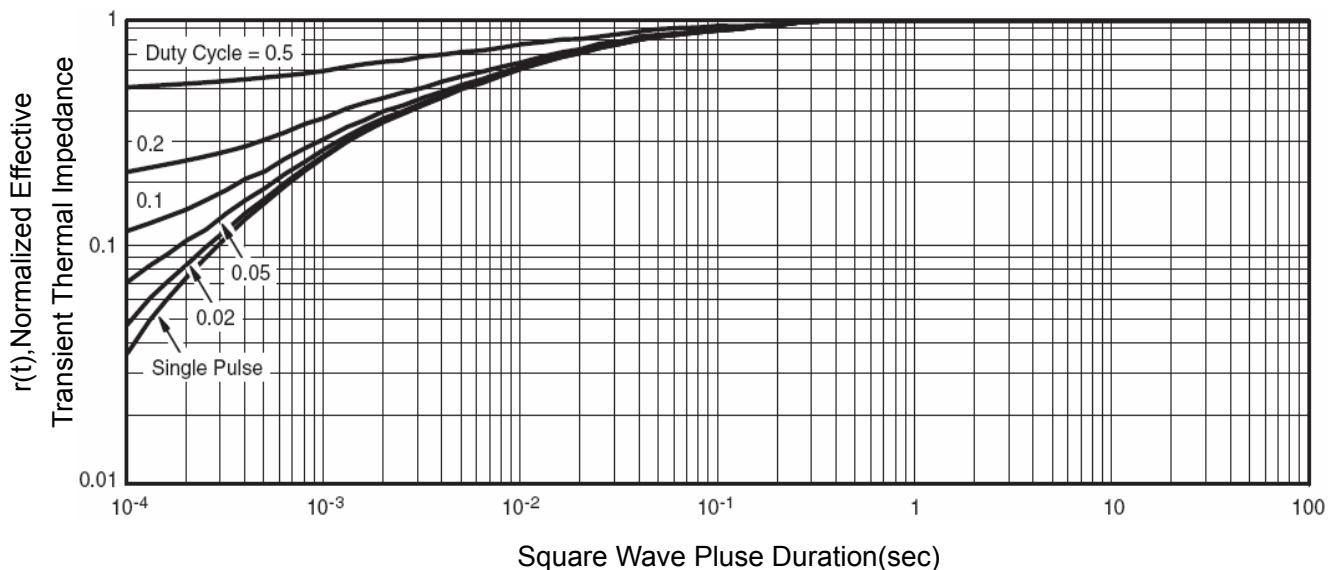
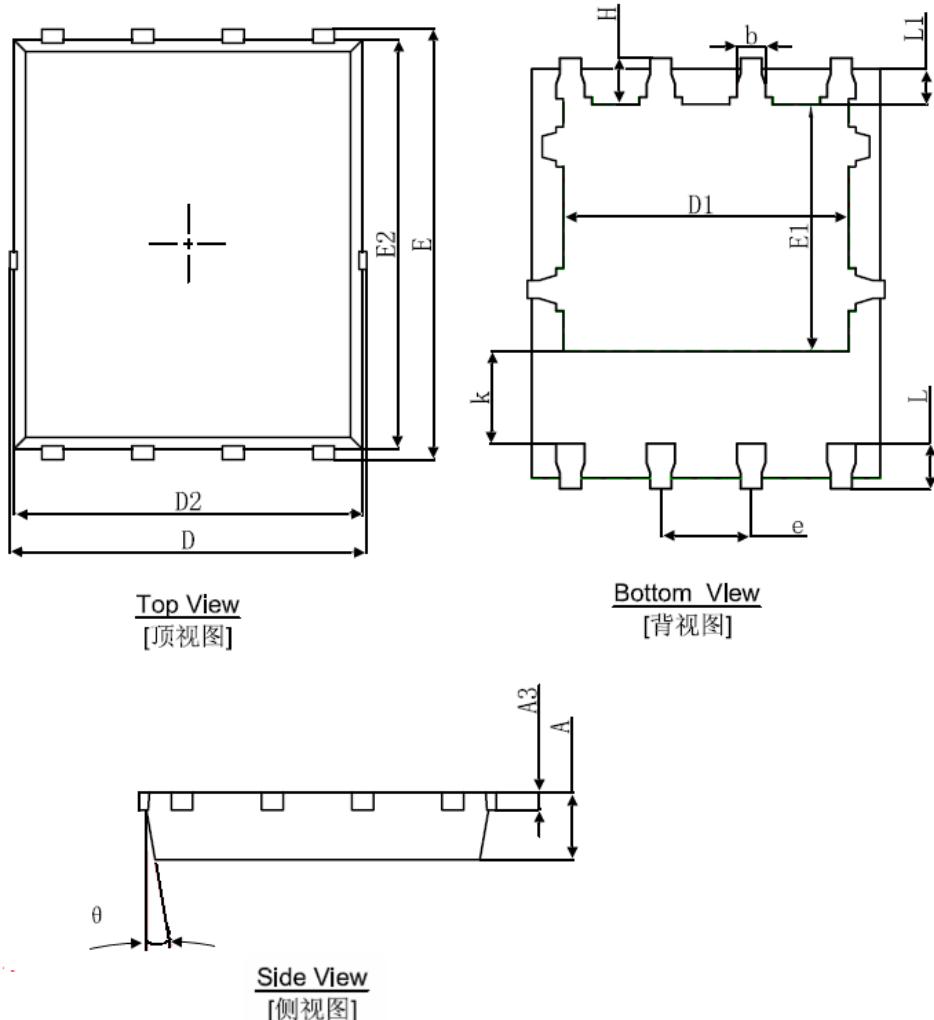


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°