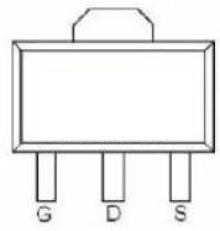
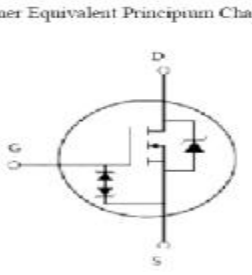
## General Description：

HM2N65PR the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is SOT--89, which accords with the RoHS standard.

| | | |
|---|---|---|
| $V_{DSS}$ | 650 | V |
| $I_D$ | 2 | A |
| $P_D(T_C=25℃)$ | 30 | W |
| $R_{DS(ON)Typ}$ | 7.8 | Ω |




SOT-89-3L top view




## Features：

- **Fast Switching**
- **ESD Improved Capability**
- **Low Gate Charge** **(Typical Data: 15nC)**
- **Low Reverse transfer capacitances(Typical: 9pF)**
- **100% Single Pulse avalanche energy Test**

## Applications：

Power switch circuit of adaptor and charger.

**Absolute**（Tc= 25℃ unless otherwise specified）：

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | 650 | V |
| $I_D$ | Continuous Drain Current | 2 | A |
| | Continuous Drain Current $T_C$ = 100 °C | 1.4 | A |
| $I_{DM}$ [a1] | Pulsed Drain Current | 6 | A |
| $V_{GS}$ | Gate-to-Source Voltage | ±30 | V |
| $E_{AS}$ [a2] | Single Pulse Avalanche Energy | 150 | mJ |
| $E_{AR}$ [a1] | Avalanche Energy ,Repetitive | 20 | mJ |
| $I_{AR}$ [a1] | Avalanche Current | 2 | A |
| dv/dt [a3] | Peak Diode Recovery dv/dt | 5.0 | V/ns |
| $P_D$ | Power Dissipation | 30 | W |
| | Derating Factor above 25°C | 0.24 | W/℃ |
| $V_{ESD(G-S)}$ | Gate source ESD (HBM-C= 100pF, R=1.5kΩ) | 3000 | V |
| $T_J$，$T_{stg}$ | Operating Junction and Storage Temperature Range | 150，–55 to 150 | ℃ |
| $T_L$ | Maximum Temperature for Soldering | 300 | ℃ |

**Electrical Characteristics**（Tc= 25℃ unless otherwise specified）：

| **OFF Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Unit |
| | | | Min. | Typ. | Max. | s |
| $V_{DSS}$ | Drain to Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250μA | 650 | -- | -- | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Bvdss Temperature Coefficient | ID=250uA,Reference25℃ | -- | 0.6 | -- | V/℃ |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{DS}$ =700V, $V_{GS}$= 0V, $T_a$ = 25℃ | -- | -- | 10 | μA |
| | | $V_{DS}$ =560V, $V_{GS}$= 0V, $T_a$ = 125℃ | -- | -- | 100 | μA |
| $I_{GSS(F)}$ | Gate to Source Forward Leakage | $V_{GS}$ =+20V | -- | -- | 10 | μA |
| $I_{GSS(R)}$ | Gate to Source Reverse Leakage | $V_{GS}$ =-20V | -- | -- | -10 | μA |

| **ON Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $R_{DS(ON)}$ | Drain-to-Source On-Resistance | $V_{GS}$=10V,$I_D$=2A | -- | 7.8 | 9.5 | Ω |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 2.0 | | 4.0 | V |
| Pulse width tp≤300μs,δ≤2% | | | | | | |

| **Dynamic Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $g_{fs}$ | Forward Trans conductance | $V_{DS}$=15V, $I_D$ =2A | | 3.5 | -- | S |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0V $V_{DS}$ = 25V f = 1.0MHz | -- | 500 | | pF |
| $C_{oss}$ | Output Capacitance | | -- | 50 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 9 | | |

| **Resistive Switching Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $t_{d(ON)}$ | Turn-on Delay Time | $I_D$ =2A $V_{DD}$ = 350V $R_G$ =25Ω | -- | 12 | -- | ns |
| tr | Rise Time | | -- | 17 | -- | |
| $t_{d(OFF)}$ | Turn-Off Delay Time | | -- | 45 | -- | |
| $t_f$ | Fall Time | | -- | 23 | -- | |
| $Q_g$ | Total Gate Charge | $I_D$ =2A $V_{DD}$ =350V $V_{GS}$ = 10V | -- | 15 | | nC |
| $Q_{gs}$ | Gate to Source Charge | | -- | 3 | | |
| $Q_{gd}$ | Gate to Drain (“Miller”)Charge | | -- | 6 | | |

| **Source-Drain Diode Characteristics** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $I_S$ | Continuous Source Current (Body Diode) | | -- | -- | 2 | A |
| $I_{SM}$ | Maximum Pulsed Current (Body Diode) | | -- | -- | 6 | A |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=2.0A,$V_{GS}$=0V | -- | -- | 1.5 | V |
| trr | Reverse Recovery Time | $I_S$=2.0A,$T_j$ = 25°C | -- | 198 | -- | ns |
| Qrr | Reverse Recovery Charge | $dI_F/dt$=100A/us, $V_{GS}$=0V | -- | 770 | -- | nC |
| Pulse width tp≤300μs,δ≤2% | | | | | | |

| Symbol | Parameter | Typ. | Units |
|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | 4.17 | ℃/W |
| $R_{\theta JA}$ | Junction-to-Ambient | 100 | ℃/W |

| **Gate-source Zener diode** | | | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Rating | | | Units |
| | | | Min. | Typ. | Max. | |
| $V_{GSO}$ | Gate-source breakdown voltage | $I_{GS}$= ±1mA(Open Drain) | 30 | | | V |
| The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components. | | | | | | |

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10mH, $I_D$=5.5A, Start $T_J$=25℃
[a3]: $I_{SD}$ =2A,di/dt ≤100A/us,$V_{DD}$≤$BV_{DS,}$ Start $T_J$=25℃

## Characteristics Curve：

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

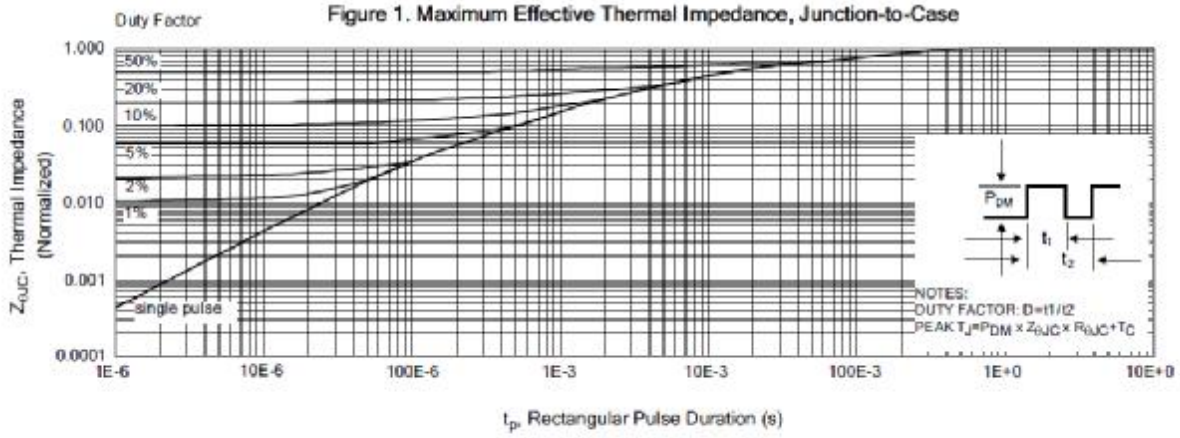



Figure 2. Maximum Power Dissipation vs Case Temperature

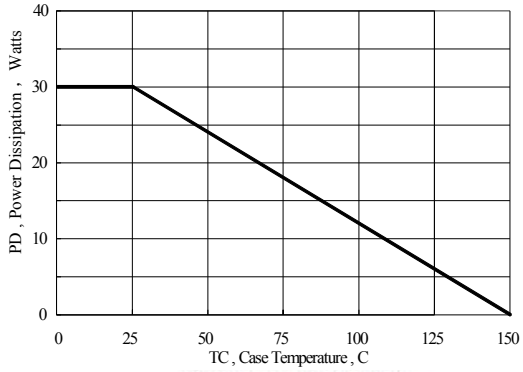



Figure 3. Maximum Continuous Drain Current vs Case Temperature

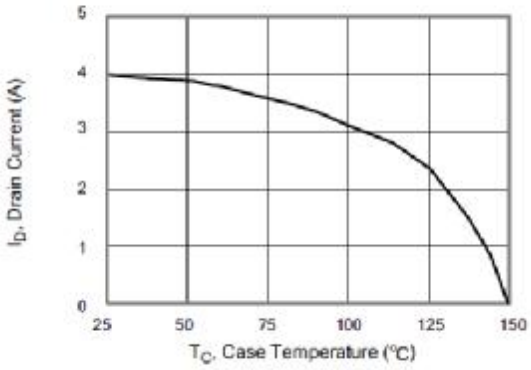



Figure 4. Typical Output Characteristics

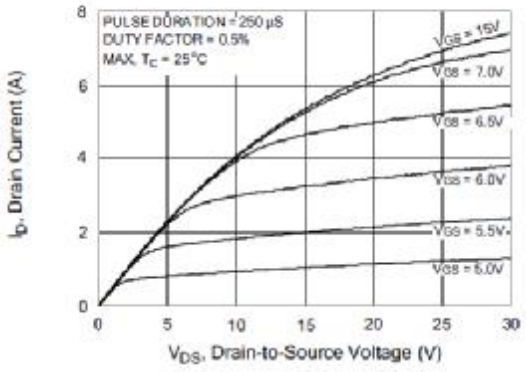



Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

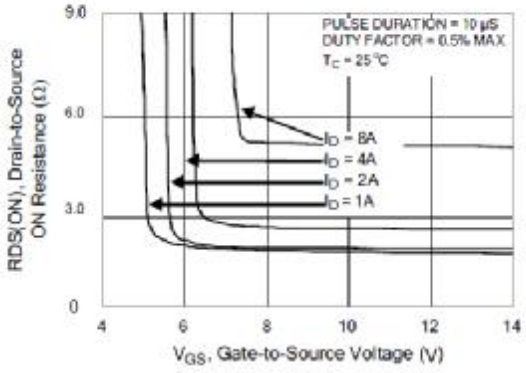


Figure 6. Maximum Peak Current Capability

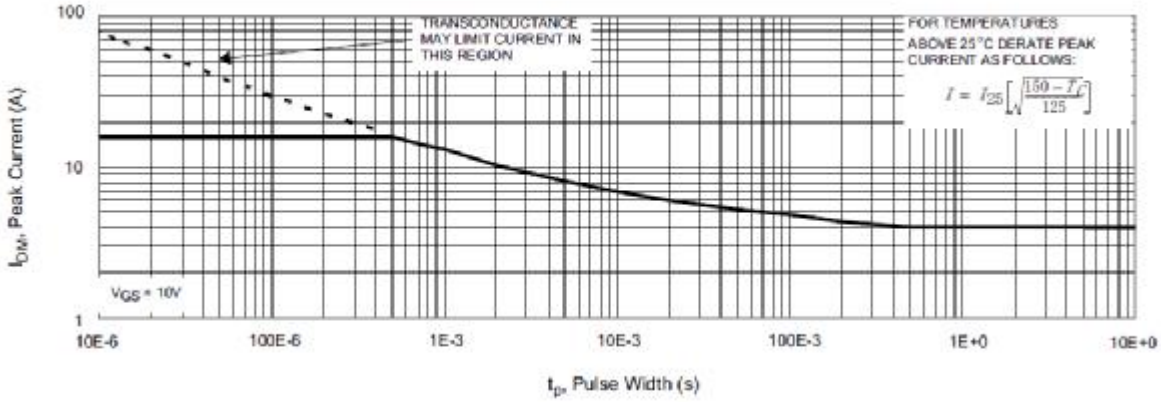



Figure 7. Typical Transfer Characteristics

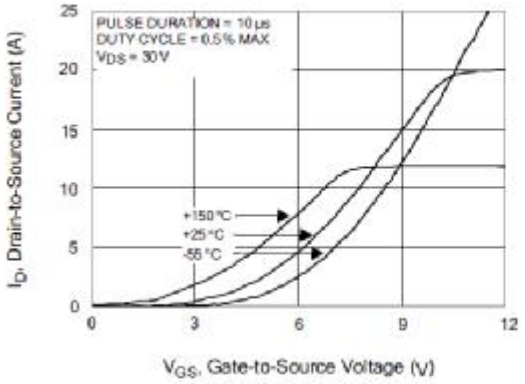



Figure 8. Unclamped Inductive Switching Capability

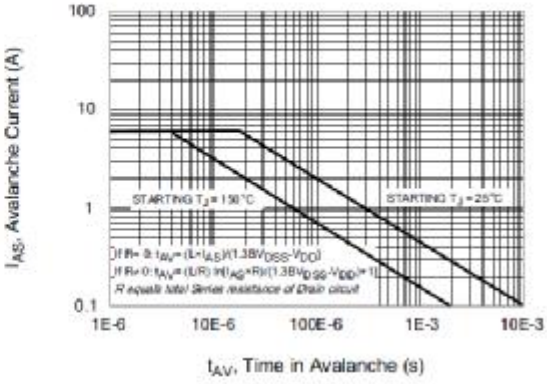



Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

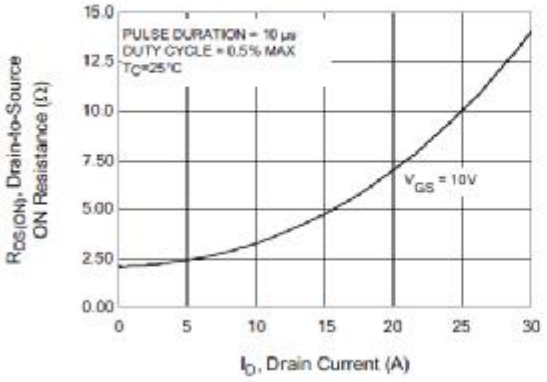



Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

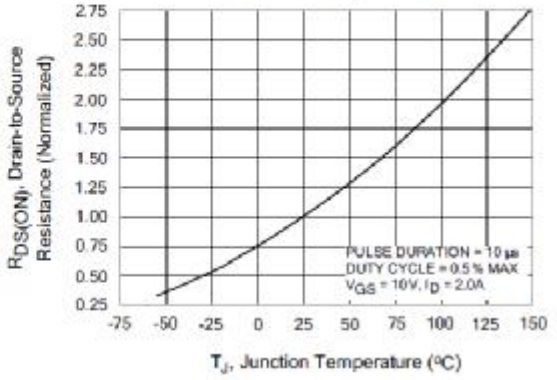


Figure 11. Typical Breakdown Voltage vs Junction Temperature

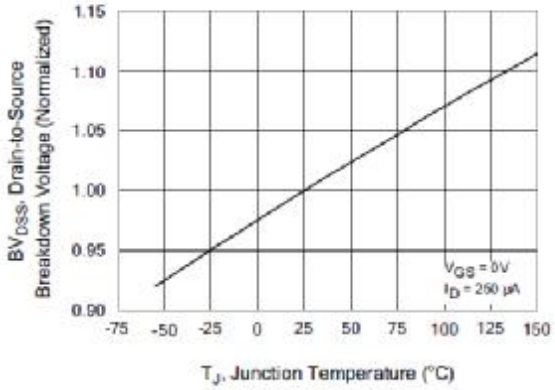



Figure 12. Typical Threshold Voltage vs Junction Temperature

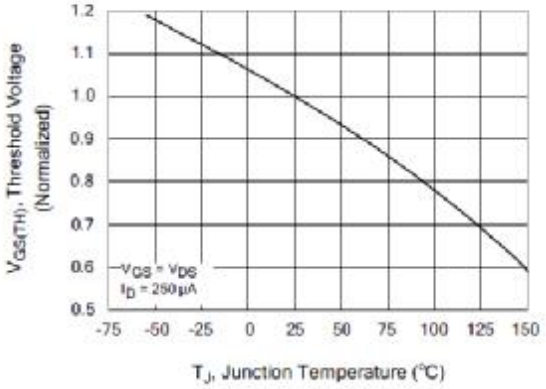



Figure 13. Maximum Forward Bias Safe Operating Area

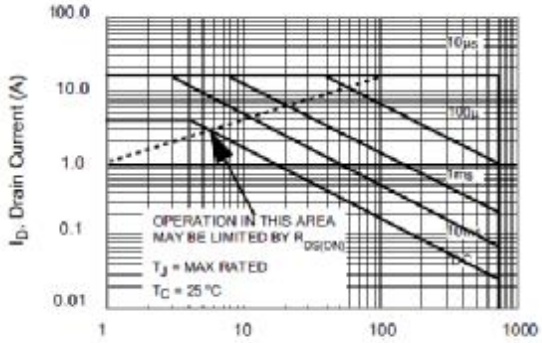



Figure 14. Typical Capacitance vs Drain-to-Source Voltage

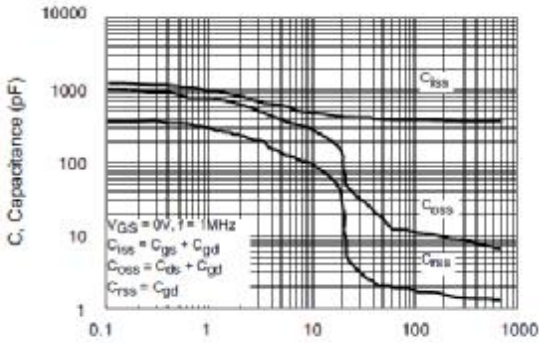



Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

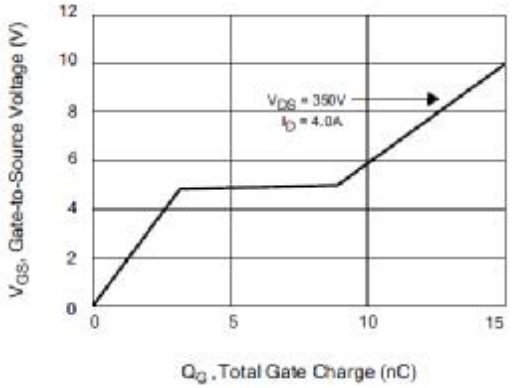
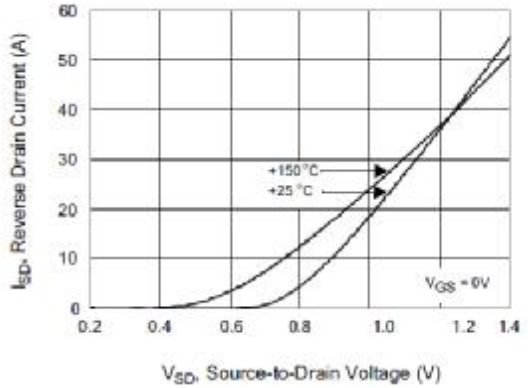



Figure 16. Typical Body Diode Transfer Characteristics



## Test Circuit and Waveform

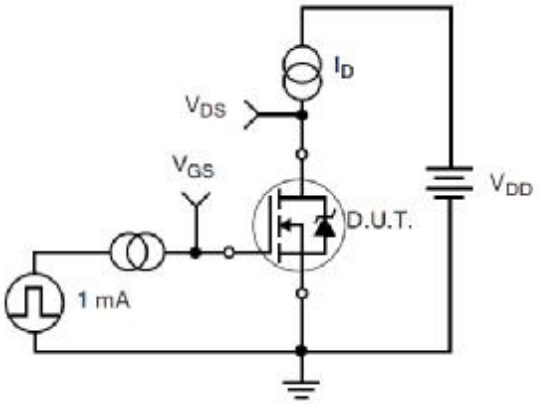



Figure 17. Gate Charge Test Circuit

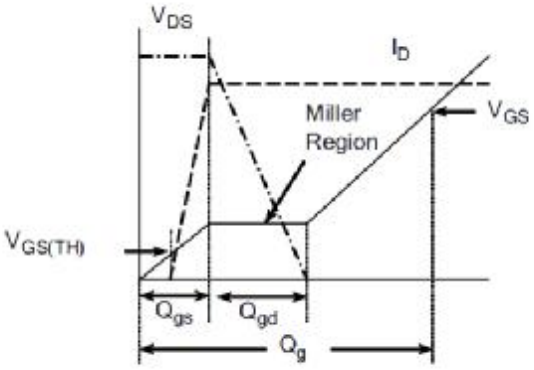



Figure 18. Gate Charge Waveform

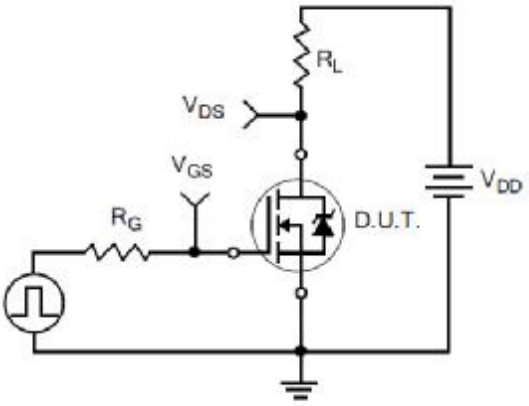



Figure 19. Resistive Switching Test Circuit

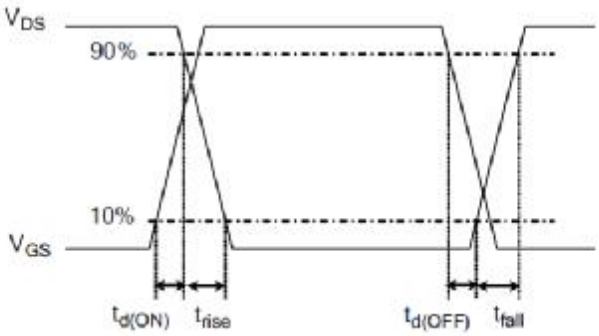



Figure 20. Resistive Switching Waveforms

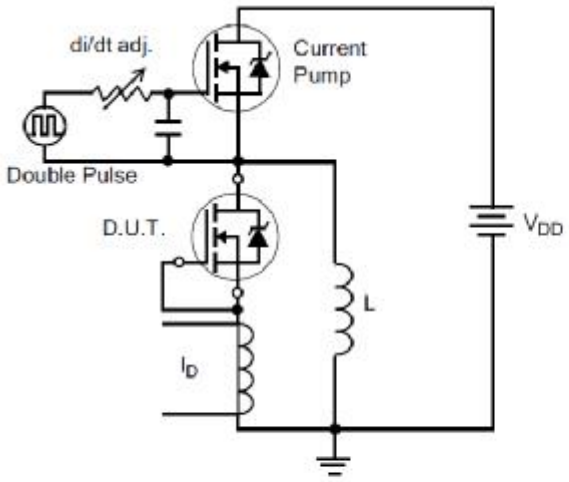



Figure 21. Diode Reverse Recovery Test Circuit

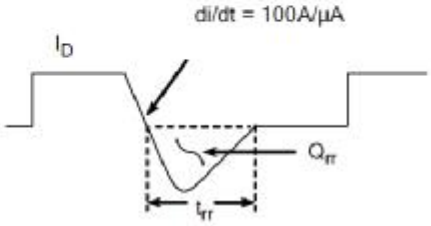



Figure 22. Diode Reverse Recovery Waveform

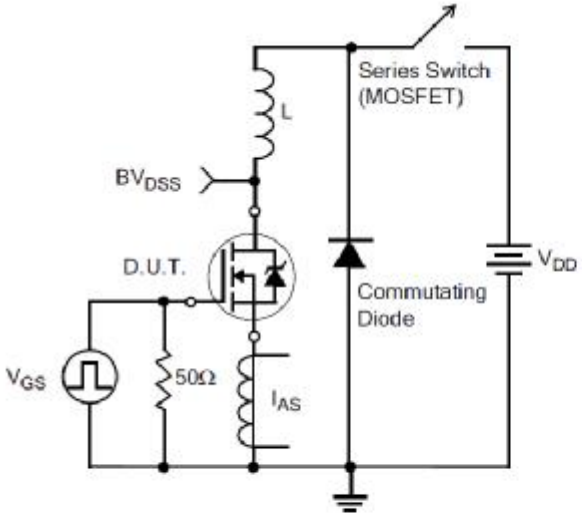



Figure 23. Unclamped Inductive Switching Test Circuit

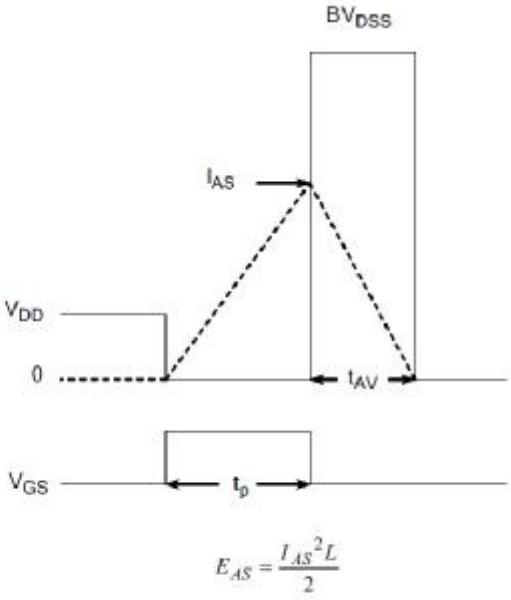
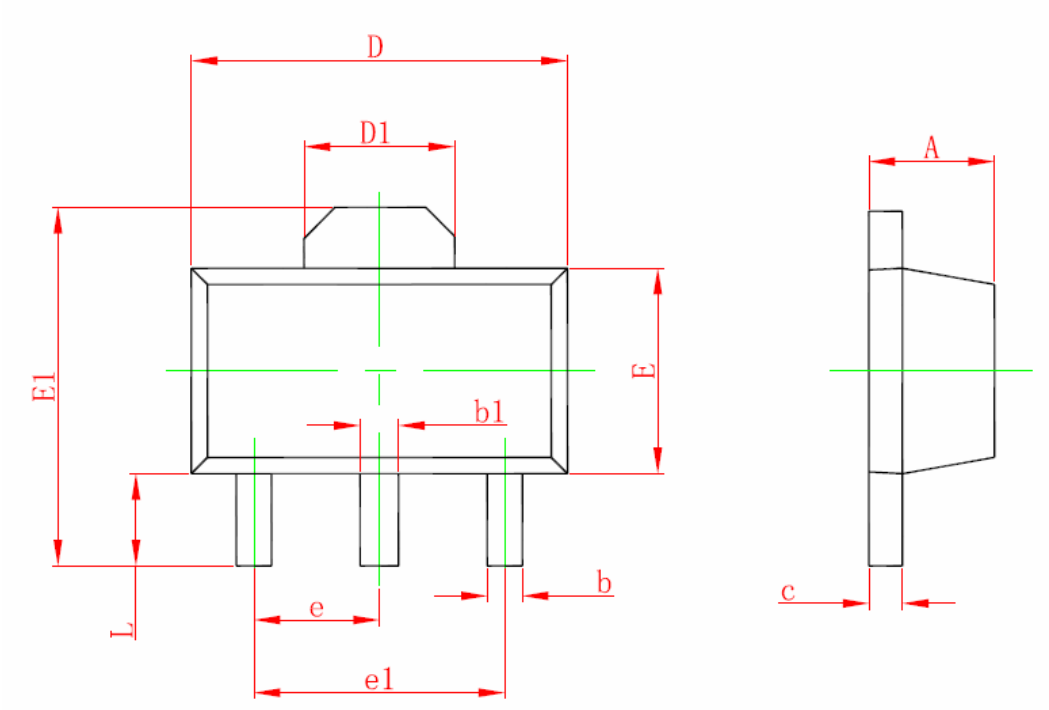



Figure 24. Unclamped Inductive Switching Waveforms

## SOT-89-3L Package Information




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.400 | 1.600 | 0.055 | 0.063 |
| b | 0.320 | 0.520 | 0.013 | 0.020 |
| b1 | 0.400 | 0.580 | 0.016 | 0.023 |
| c | 0.350 | 0.440 | 0.014 | 0.017 |
| D | 4.400 | 4.600 | 0.173 | 0.181 |
| D1 | 1.550 REF. | | 0.061 REF. | |
| E | 2.300 | 2.600 | 0.091 | 0.102 |
| E1 | 3.940 | 4.250 | 0.155 | 0.167 |
| e | 1.500 TYP. | | 0.060 TYP. | |
| e1 | 3.000 TYP. | | 0.118 TYP. | |
| L | 0.900 | 1.200 | 0.035 | 0.047 |

## Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

**The name and content of poisonous and harmful material in products**

| Part's Name | Hazardous Substance | | | | | |
|---|---|---|---|---|---|---|
| | Pb | Hg | Cd | Cr(VI) | PBB | PBDE |
| Limit | ≤0.1% | ≤0.1% | ≤0.01% | ≤0.1% | ≤0.1% | ≤0.1% |
| Lead Frame | ○ | ○ | ○ | ○ | ○ | ○ |
| Molding Compound | ○ | ○ | ○ | ○ | ○ | ○ |
| Chip | ○ | ○ | ○ | ○ | ○ | ○ |
| Wire Bonding | ○ | ○ | ○ | ○ | ○ | ○ |
| Solder | × | ○ | ○ | ○ | ○ | ○ |
| Note | ○：means the hazardous material is under the criterion of SJ/T11363-2006.<br>×：means the hazardous material exceeds the criterion of SJ/T11363-2006.<br>The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS. | | | | | |

## Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heatsink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by H&M Semiconductor and subject to regular change without notice.