

P-Channel Enhancement Mode Power MOSFET

Description

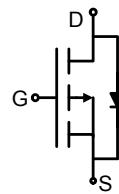
The HM20P02Q uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

General Features

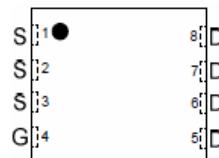
- $V_{DS} = -20V, I_D = -20A$
- $R_{DS(ON)} < 28m\Omega @ V_{GS}=-4.5V$
- $R_{DS(ON)} < 40m\Omega @ V_{GS}=-2.5V$
- High power and current handling capability
- Lead free product is acquired
- Surface Mount Package

Application

- Motor drive
- Load switch
- Power management



Schematic diagram



Pin Assignment



DFN 3.3x3.3 EP top view

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM20P02Q	HM20P02Q	DFN3X3-8L	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	-20	A
Drain Current-Pulsed (Note 1)	I_{DM}	-60	A
Maximum Power Dissipation	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	42	$^\circ C/W$
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Electrical Characteristics ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V I_D=-250\mu A$	-20	-	-	V

Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.5	-0.7	-1.4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-6A	-	22	28	mΩ
		V _{GS} =-2.5V, I _D =-5A		32	40	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-15V, I _D =-6A	-	17	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, F=1.0MHz	-	2100	-	PF
Output Capacitance	C _{oss}		-	498	-	PF
Reverse Transfer Capacitance	C _{rss}		-	300	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-10V, R _L =10Ω, V _{GS} =-4.5V, R _{GEN} =6Ω	-	25	-	nS
Turn-on Rise Time	t _r		-	30	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	50	-	nS
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-6A, V _{GS} =-4.5V	-	17	-	nC
Gate-Source Charge	Q _{gs}		-	4.1	-	nC
Gate-Drain Charge	Q _{gd}		-	4.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V, I _S =-20A	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

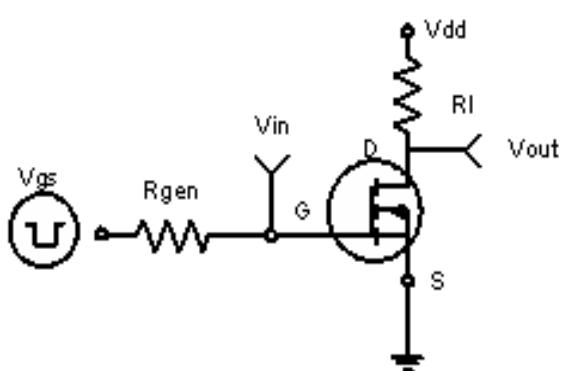


Figure 1 Switching Test Circuit

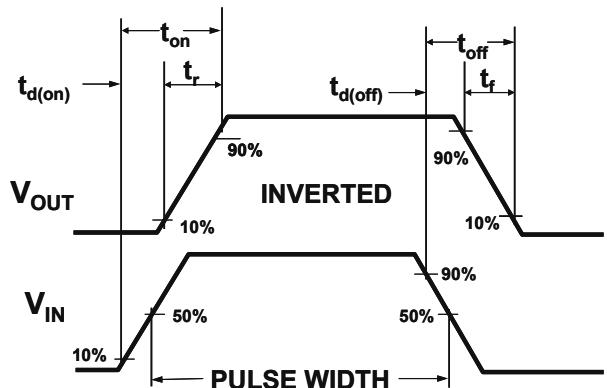


Figure 2 Switching Waveforms

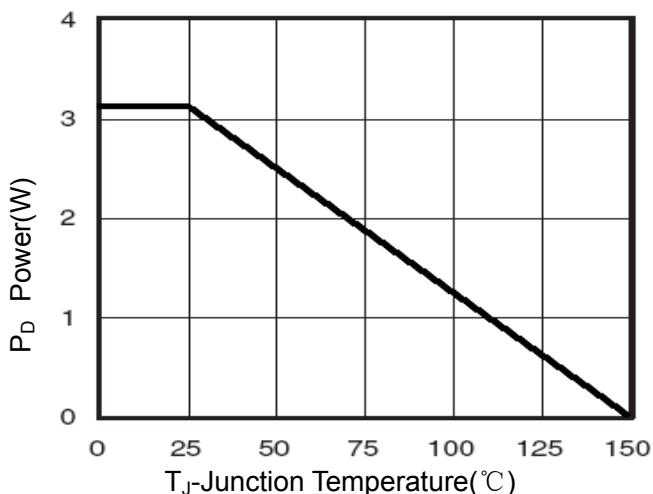


Figure 3 Power Dissipation

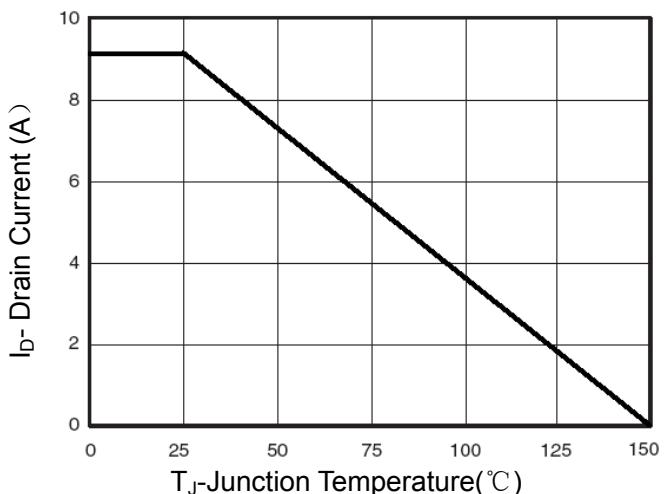


Figure 4 Drain Current

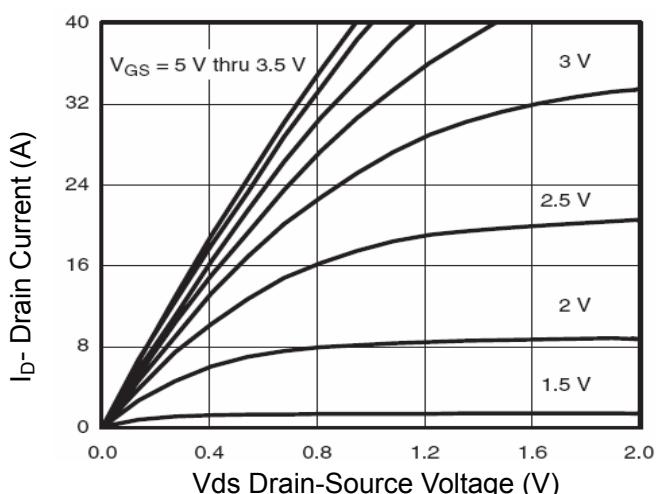


Figure 5 Output Characteristics

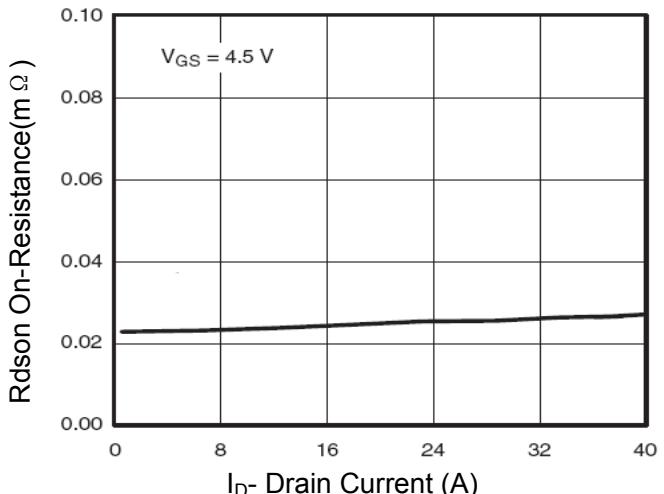


Figure 6 Drain-Source On-Resistance

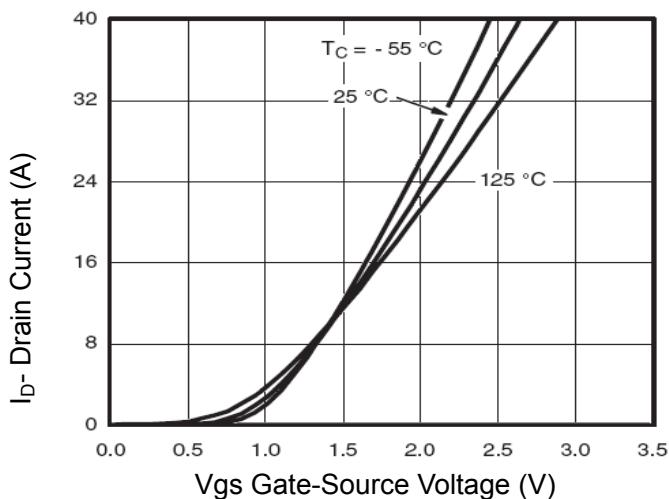


Figure 7 Transfer Characteristics

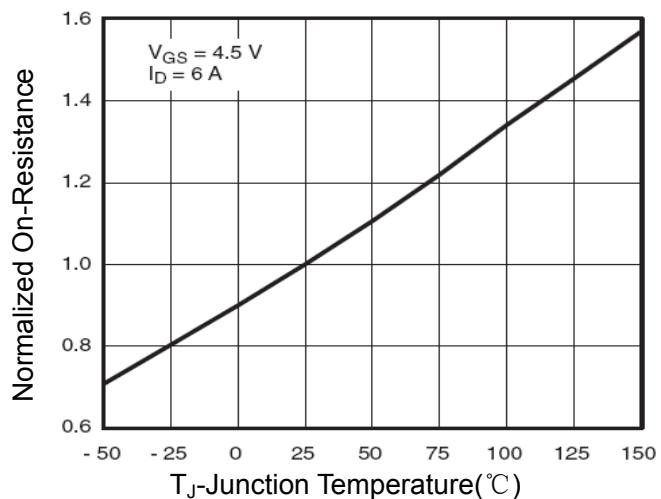


Figure 8 Drain-Source On-Resistance

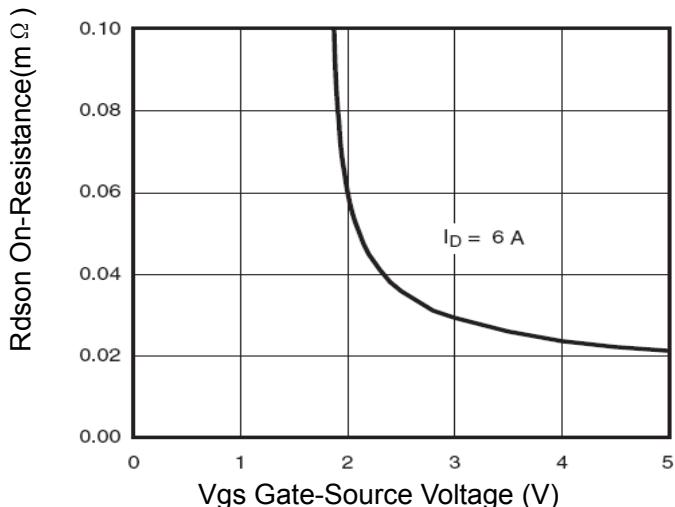


Figure 9 $R_{DS(on)}$ vs V_{GS}

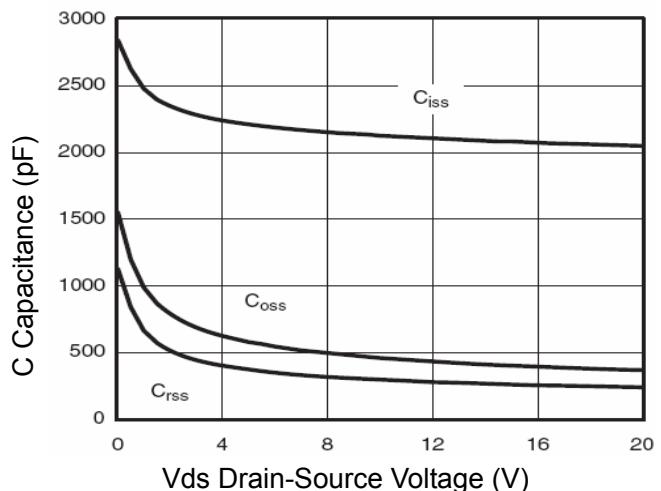


Figure 10 Capacitance vs V_{DS}

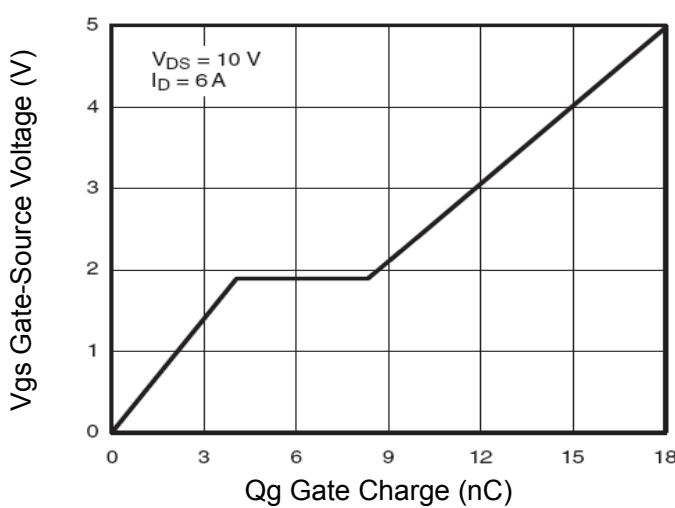


Figure 11 Gate Charge

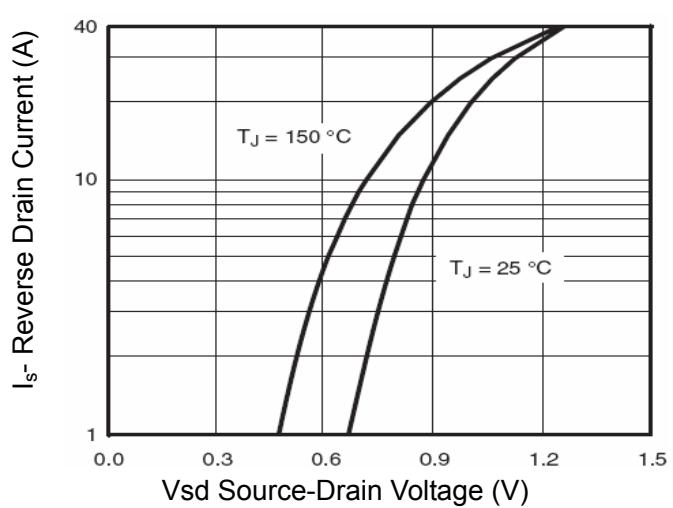


Figure 12 Source-Drain Diode Forward

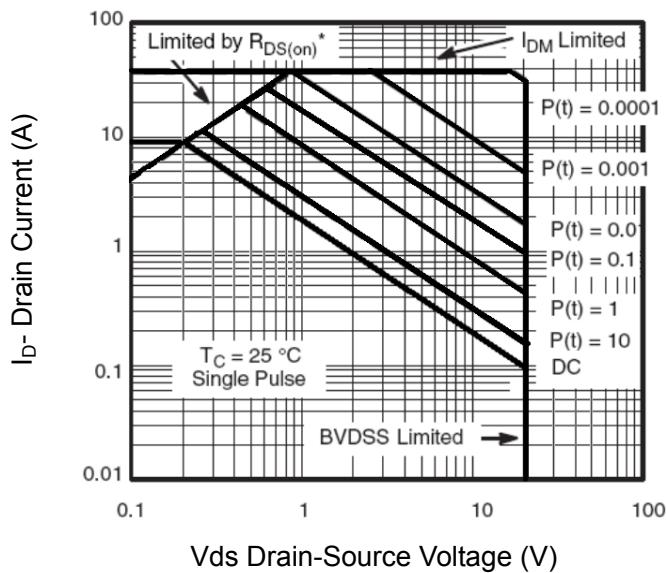


Figure 13 Safe Operation Area

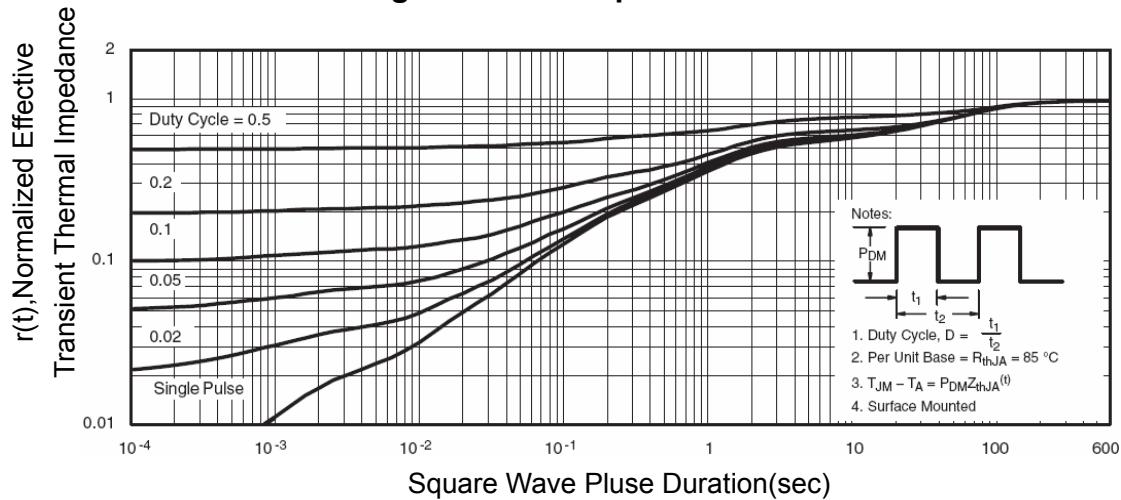


Figure 14 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3 EP Package Information

封装外形尺寸图			
符号	单位: mm		
	MIN	MAX	TYP
A	0.75	0.85	0.8
B	0.25	0.35	0.3
C	0.18	0.22	0.2
D	3.2	3.3	3.25
E	3.2	3.3	3.25
F	2.2	2.5	2.35
G	1.8	2.0	1.9
H	0.3	0.4	0.35
I	0.15	0.25	0.2
J	0.4	0.5	0.45
K	0.6	0.7	0.65
L	1.38	1.58	1.48
M	1.8	2.1	1.95
N	0.15*45°		
O	0.4	0.5	0.45

