N-Channel Enhancement Mode Power MOSFET

Description

The HM100N03GA uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

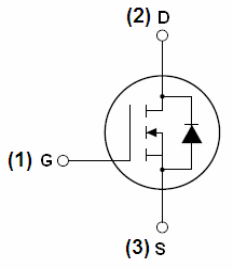
General Features

- V_{DS} =30V,I_D =100A
  $R_{DS(ON)}$ = 3.6mΩ (typical) @ VGS=10V
  $R_{DS(ON)}$ = 5.2mΩ (typical) @ VGS=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

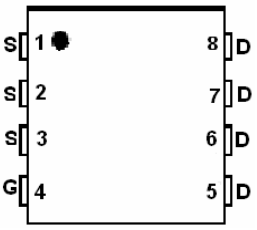
Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!



Schematic diagram



Marking and pin assignment

DFN5X6-8L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM100N03GA	HM100N03GA	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	70	A
Pulsed Drain Current	I_{DM}	300	A
Maximum Power Dissipation	P_D	83	W
Derating factor		0.56	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	306	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.8	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

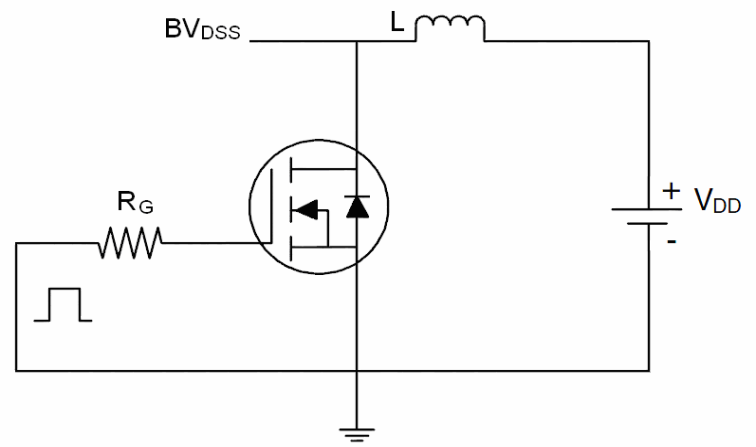
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	3.6	4.5	mΩ
		V_{GS}=4.5V, I_D=24A	-	5.6	7.5	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=24A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	2330	-	PF
Output Capacitance	C_{oss}		-	460	-	PF
Reverse Transfer Capacitance	C_{rss}		-	230	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,I_D=30A V_{GS}=10V,R_{GEN}=2.7Ω	-	20	-	nS
Turn-on Rise Time	t_r		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=30A, V_{GS}=10V	-	51	-	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain Charge	Q_{gd}		-	11	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=24A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	100	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 30A di/dt = 100A/μs (Note3)	-	32	50	nS
Reverse Recovery Charge	Qrr		-	12	20	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

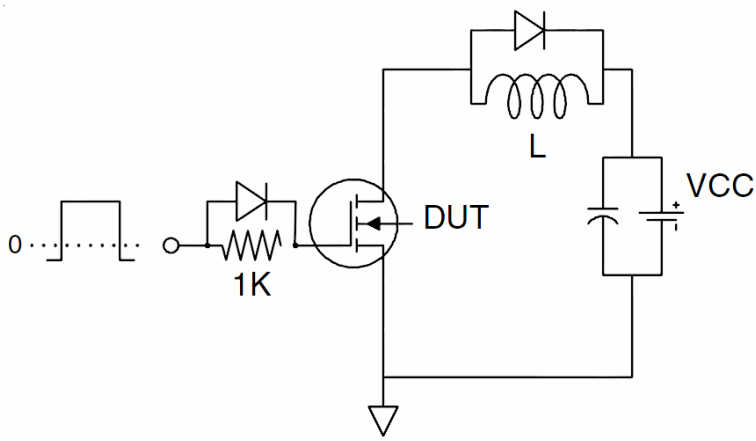
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω，I_{AS}=35A

Test Circuit

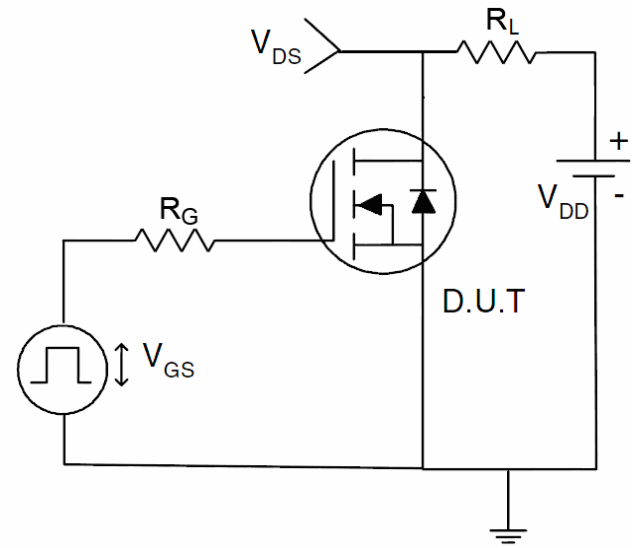
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

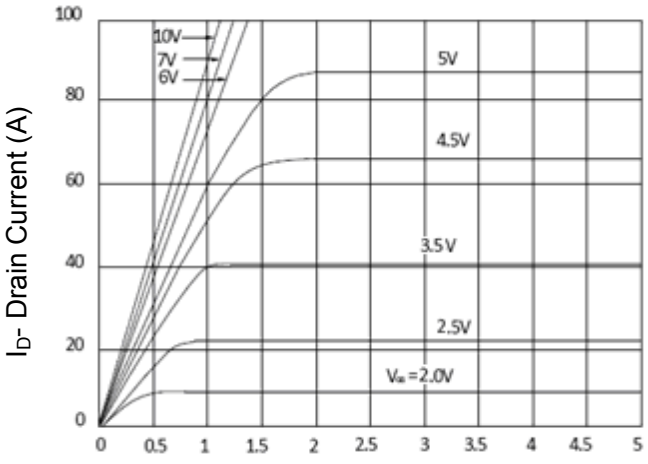


Figure 1 Output Characteristics

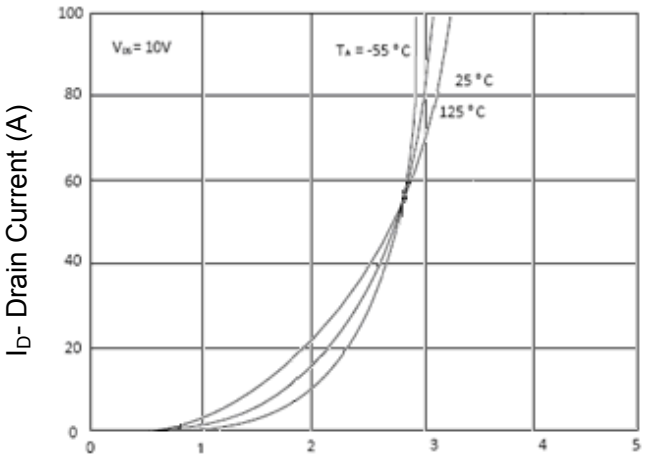


Figure 2 Transfer Characteristics

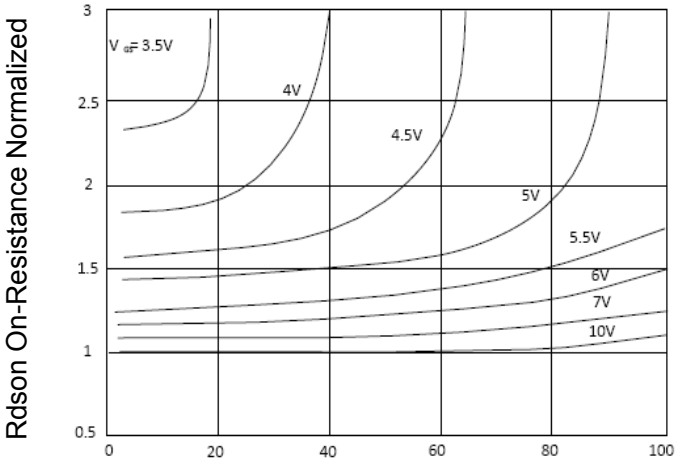


Figure 3 Rdson- Drain Current

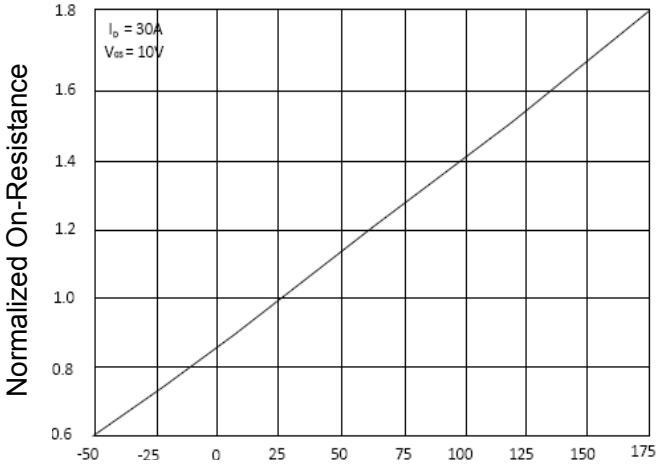


Figure 4 Rdson-Junction Temperature

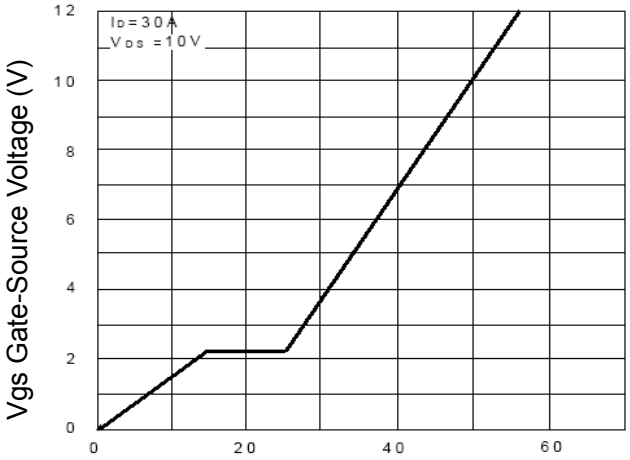


Figure 5 Gate Charge

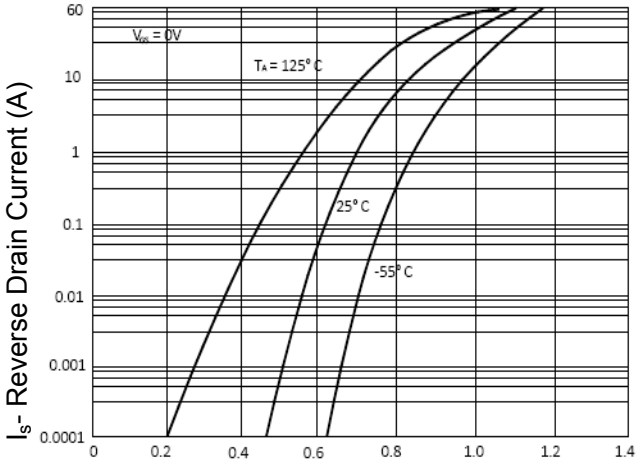


Figure 6 Source- Drain Diode Forward

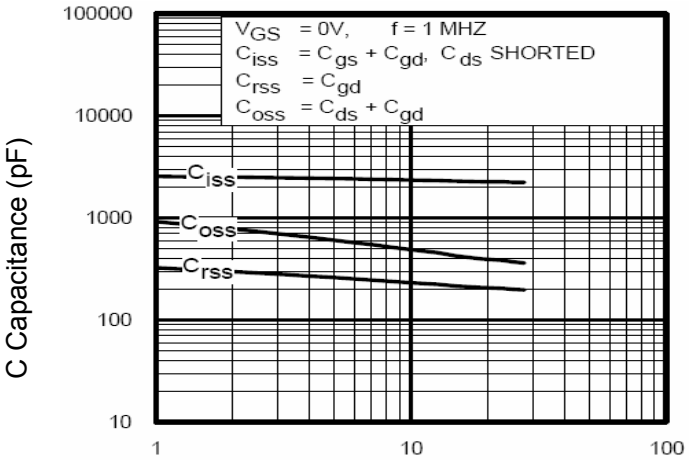


Figure 7 Capacitance vs Vds

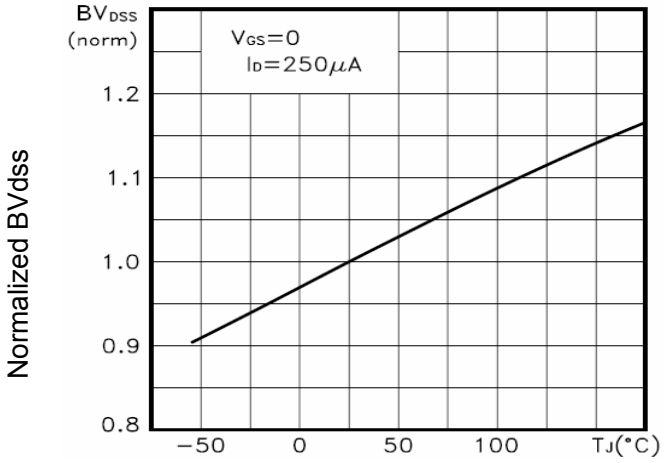


Figure 9 BV_{DSS} vs Junction Temperature

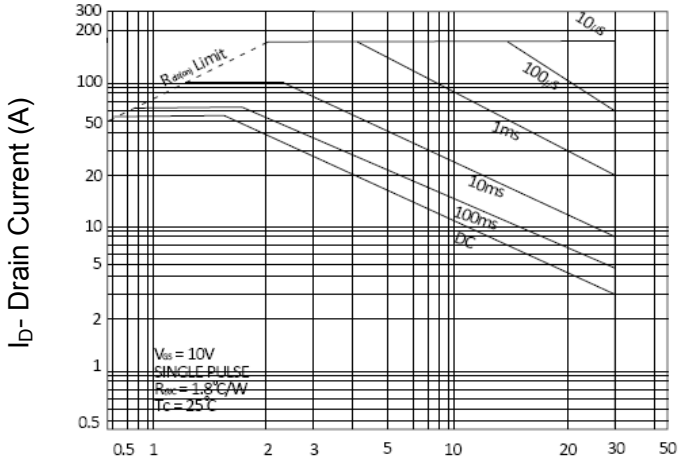


Figure 8 Safe Operation Area

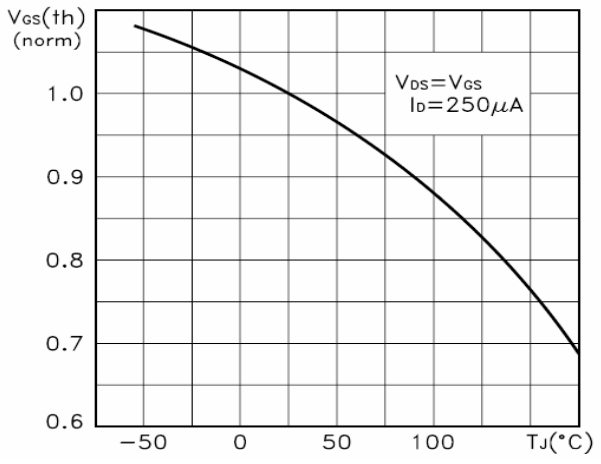


Figure 10 $V_{GS(th)}$ vs Junction Temperature

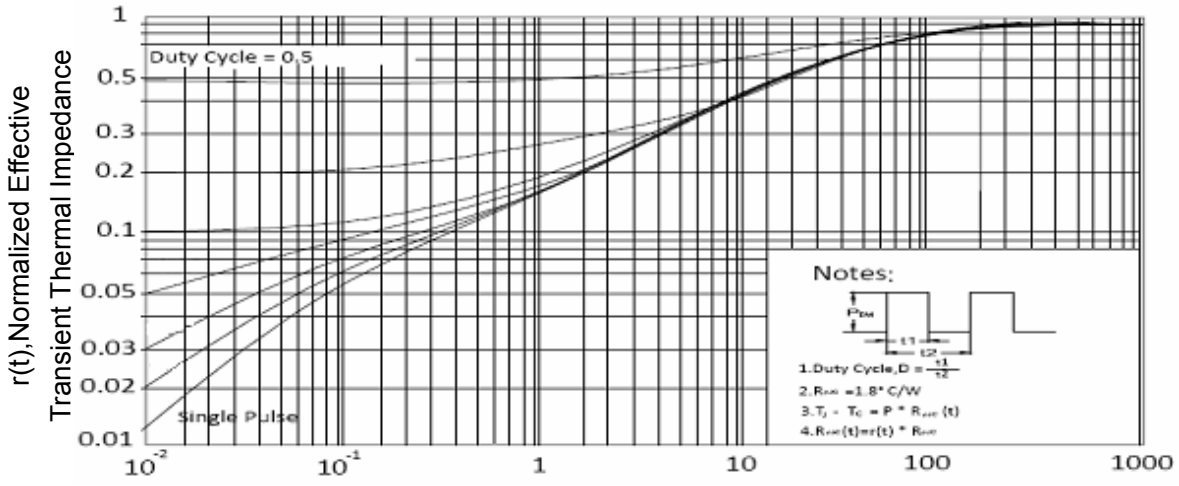
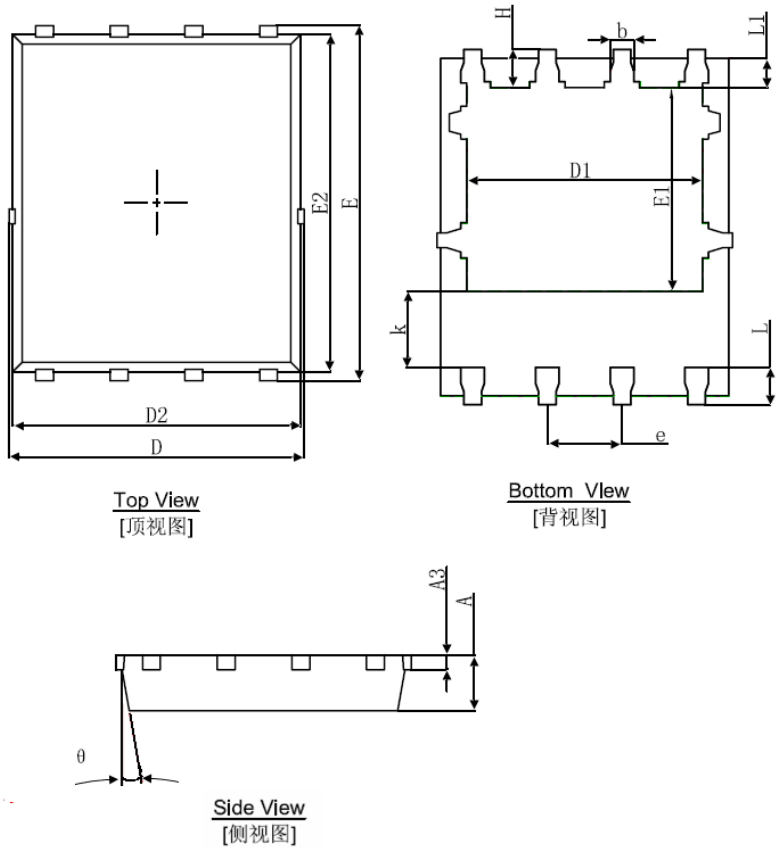


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°