

HMS5N65K
650V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)} \times Q_g$)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

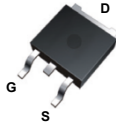
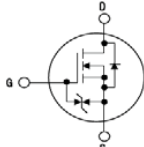
Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power
- AC to DC Converters
- Telecom

Key Parameters

Parameter	Value	Unit
$BV_{DSS} @T_{j,max}$	750	V
I_D	5.0	A
$R_{DS(on), max}$	1.1	Ω
Qg, Typ	9.3	nC

Package & Internal Circuit

D-PAK	SYMBOL
	

Absolute Maximum Ratings $T_C=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous ($T_C = 25^{\circ}C$)	5.0	A
	Drain Current - Continuous ($T_C = 100^{\circ}C$)	3.5	A
$I_{DM}^{1)}$	Drain Current - Pulsed	15.0	A
$E_{AS}^{2)}$	Single Pulsed Avalanche Energy	35	mJ
I_{AR}	Avalanche Current	0.9	A
dv/dt	MOSFET dv/dt ruggedness, $V_{DS}=0 \dots 400V$	50	V/ns
dv/dt	Reverse diode dv/dt, $V_{DS}=0 \dots 400V, I_{DS} \leq I_D$	15	V/ns
P_D	Power Dissipation ($T_C = 25^{\circ}C$)	50	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^{\circ}C$

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient , Max.	62.5	$^{\circ}C/W$

Electrical Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V _{GS}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 140 μA	2.0	-	4.0	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 1.2 A (CHIP) (PACKAGE)	-	957 870	1100 1000	mΩ
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1mA	650	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0	-	-	1	μA
		V _{DS} = 650 V, T _C = 150°C	-	-	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C _{iSS}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1.0 MHz	-	410	-	pF
C _{oSS}	Output Capacitance		-	13	-	pF
C _{rSS}	Reverse Transfer Capacitance		-	2.7	-	pF
Switching Characteristics						
t _{d(on)}	Turn-On Time	V _{DS} = 350 V, I _D = 1.8 A, R _G = 25 Ω (Note 3,4)	-	20	-	ns
t _r	Turn-On Rise Time		-	18	-	ns
t _{d(off)}	Turn-Off Delay Time		-	54	-	ns
t _f	Turn-Off Fall Time		-	19	-	ns
Q _{g(}	Total Gate Charge	V _{DS} = 560 V, I _D = 1.8 A, V _{GS} = 10 V (Note 3,4)	-	9.3	-	nC
Q _{gs}	Gate-Source Charge		-	1.8	-	nC
Q _{gd}	Gate-Drain Charge		-	3.0	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	5.0	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	15.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.8 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _R = 400 V, I _F = 1.8 A di _F /dt = 100 A/μs	-	210	-	ns
Q _{rr}	Reverse Recovery Charge		-	1.2	-	μC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=0.9\text{A}$ $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics

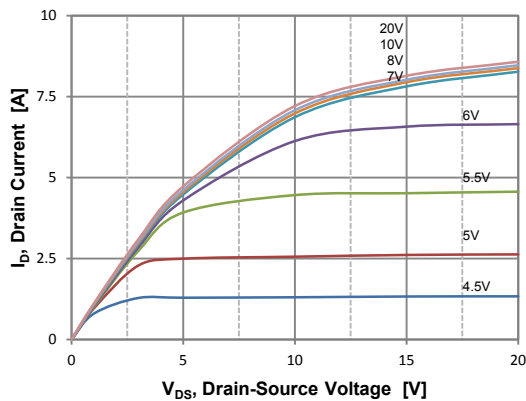


Figure 1. On Region Characteristics

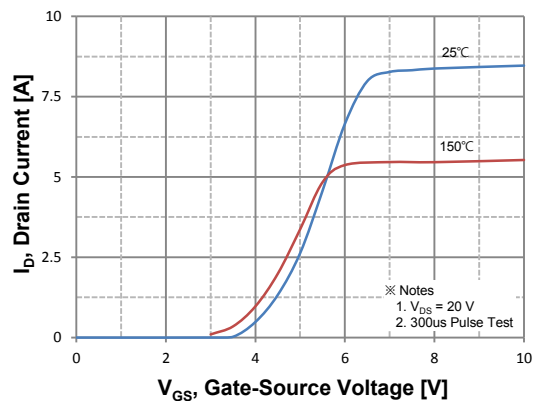


Figure 2. Transfer Characteristics

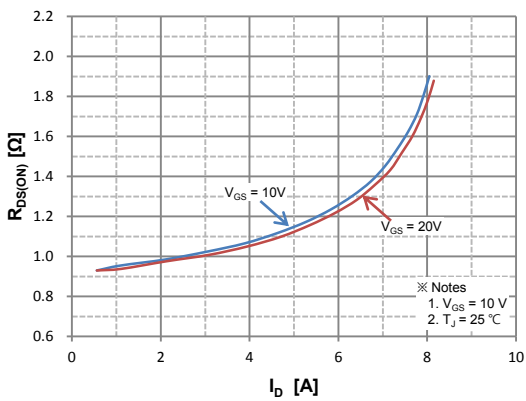


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

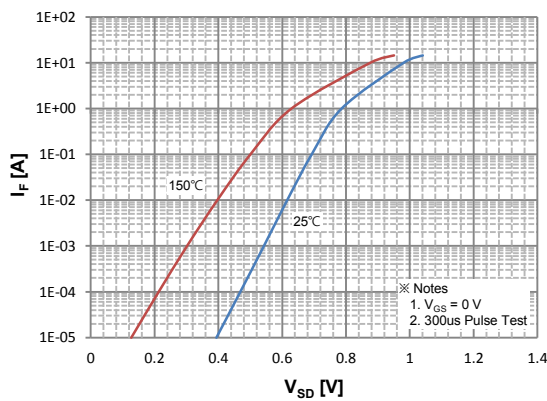


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

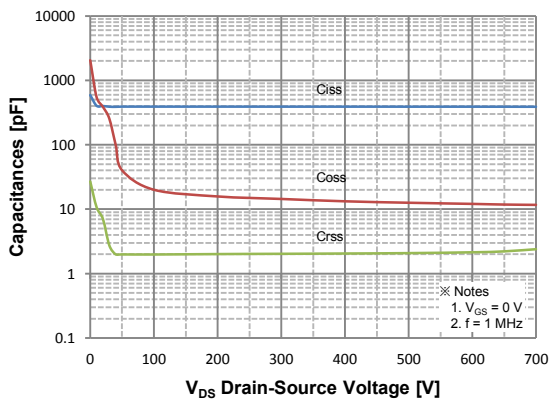


Figure 5. Capacitance Characteristics

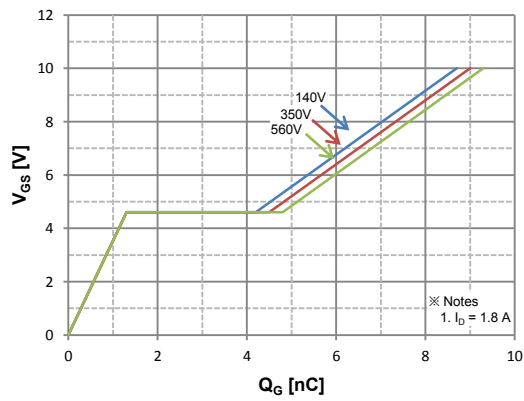


Figure 6. Gate Charge Characteristics

Typical Characteristics

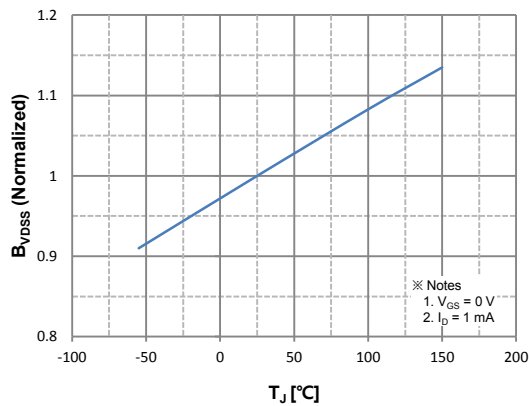


Figure 7. Breakdown Voltage Variation vs. Temperature

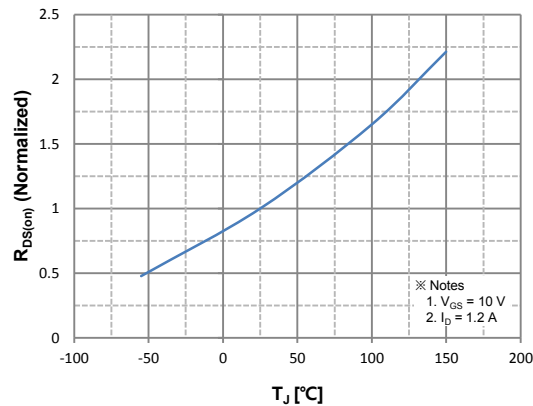


Figure 8. On-Resistance Variation vs. Temperature

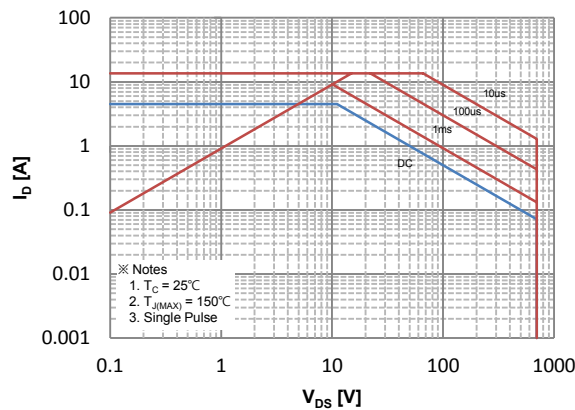


Figure 9. Maximum Safe Operating Area

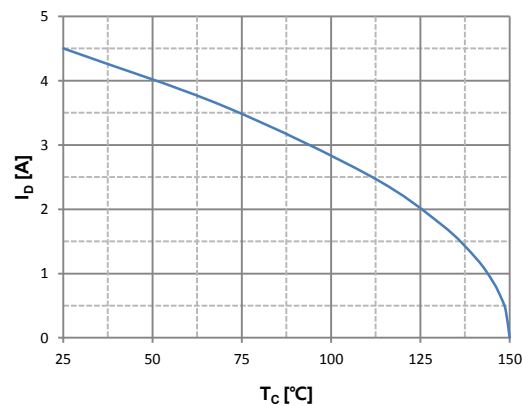


Figure 10. Maximum Drain Current vs. Case Temperature

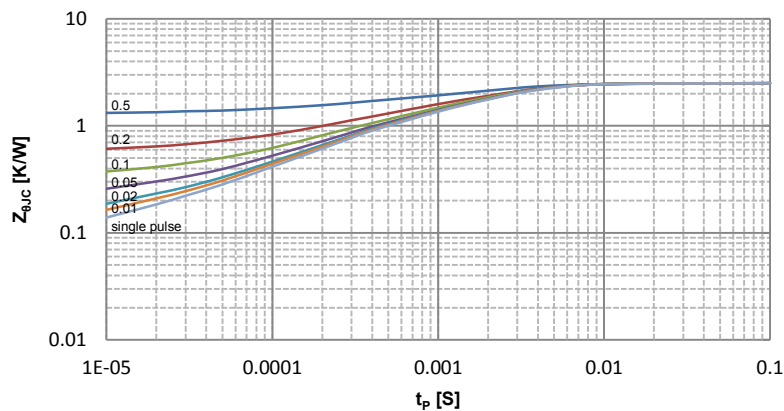


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

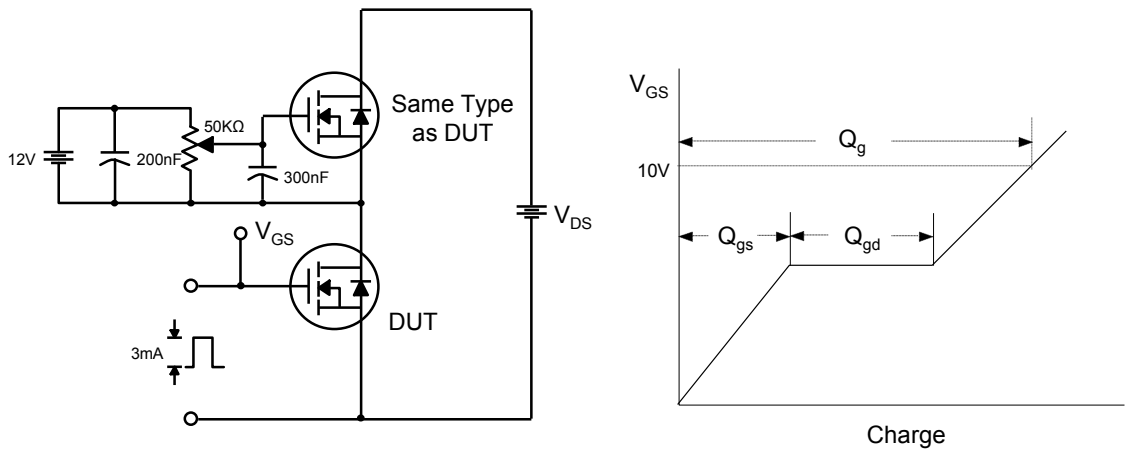


Fig 13. Resistive Switching Test Circuit & Waveforms

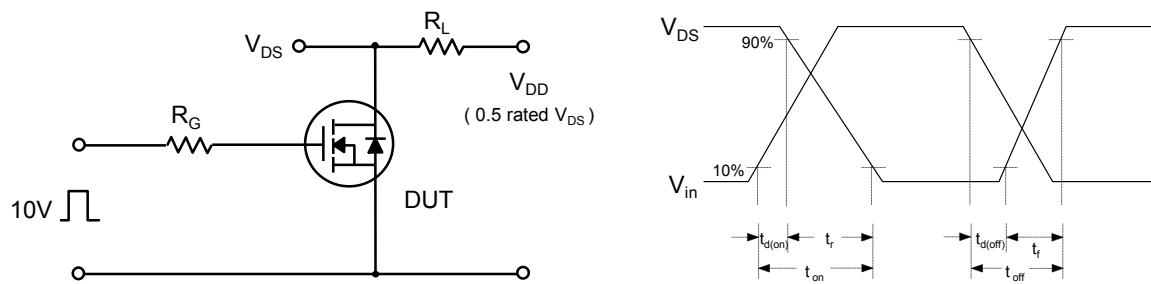


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

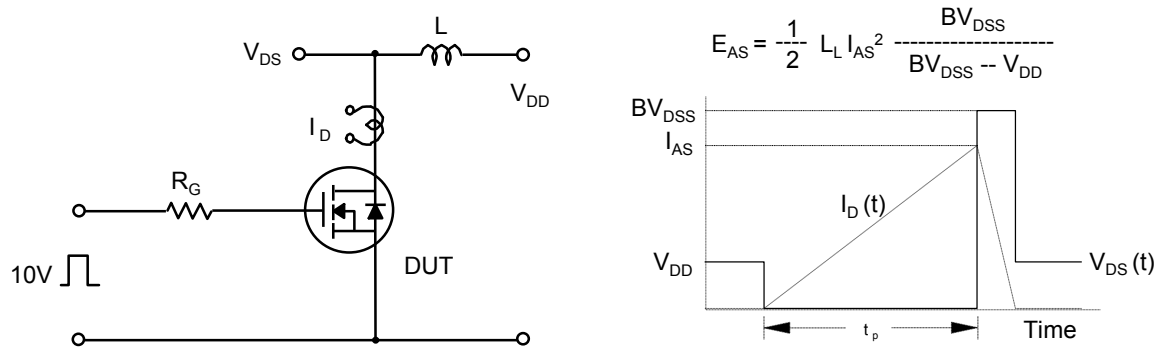
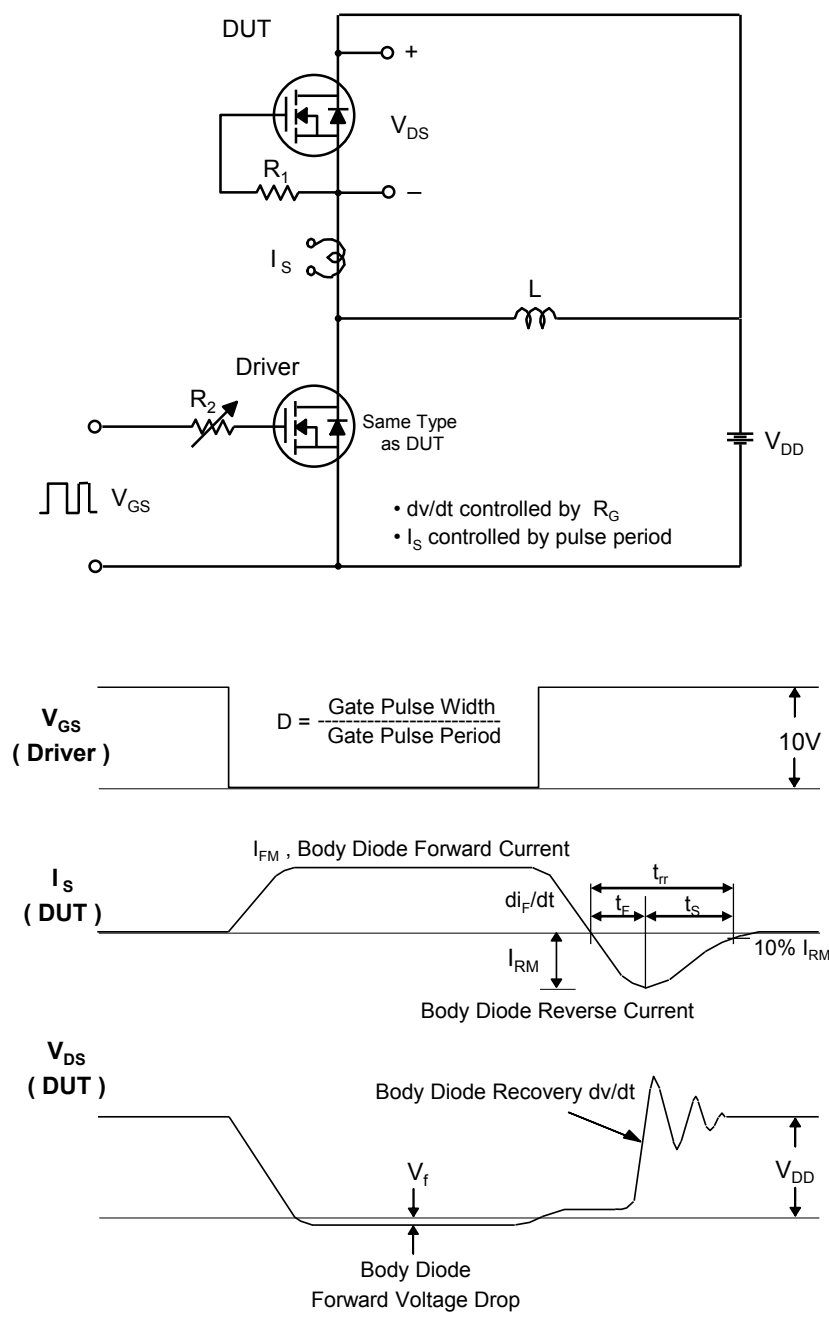


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)

