

Dual P-Channel Enhancement Mode Power MOSFET

Description

The HM4821A uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for high current load applications.

General Features

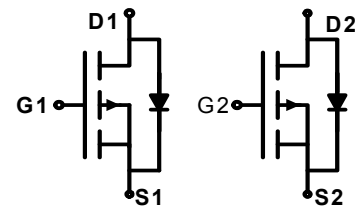
- $V_{DS} = -60V, I_D = -9A$
 $R_{DS(ON)} < 32m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

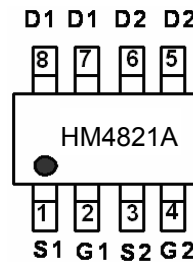
- Load switch

100% UIS TESTED!

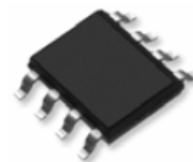
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4821A	HM4821A	SOP8	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-9	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	-6.3	A
Pulsed Drain Current	I_{DM}	-27	A
Maximum Power Dissipation	P_D	3	W
Derating factor		0.76	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	722	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.31	$^\circ\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

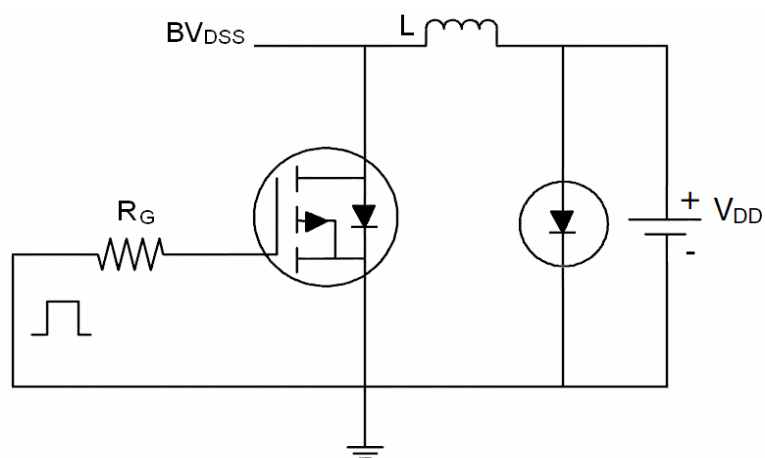
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-2.0	-2.6	-3.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-9A	-	25	32	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-9A	-	25	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V, F=1.0MHz	-	6460	-	PF
Output Capacitance	C _{oss}		-	719	-	PF
Reverse Transfer Capacitance	C _{rss}		-	535	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V, R _L =1.5Ω, V _{GS} =-10V, R _G =3Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	17	-	nS
Turn-Off Delay Time	t _{d(off)}		-	40	-	nS
Turn-Off Fall Time	t _f		-	45	-	nS
Total Gate Charge	Q _g	V _{DS} =-30, I _D =-9A, V _{GS} =-10V	-	75		nC
Gate-Source Charge	Q _{gs}		-	16		nC
Gate-Drain Charge	Q _{gd}		-	19		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-9A	-		-1.2	V
Diode Forward Current (Note 2)	I _S		-	-	-9	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =- 9A di/dt = -100A/μs(Note3)	-	50		nS
Reverse Recovery Charge	Q _{rr}		-	59		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

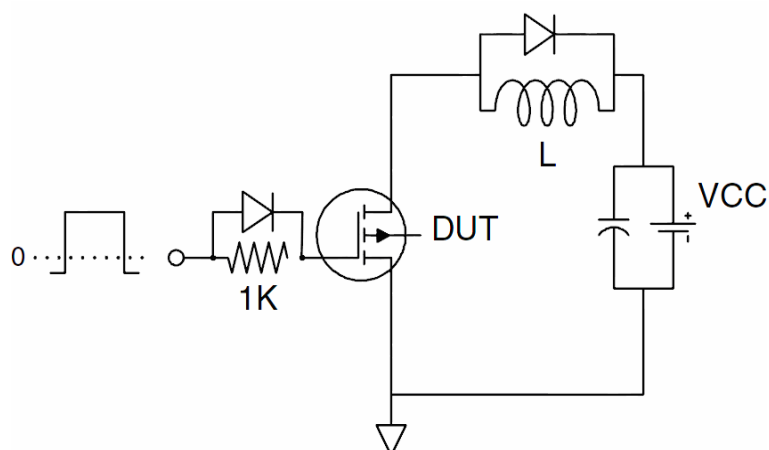
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_g=25\Omega, I_{AS}=38A$

Test Circuit

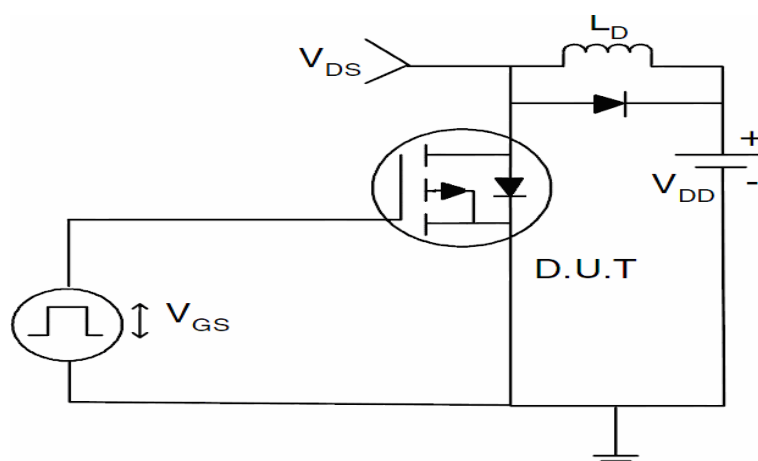
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

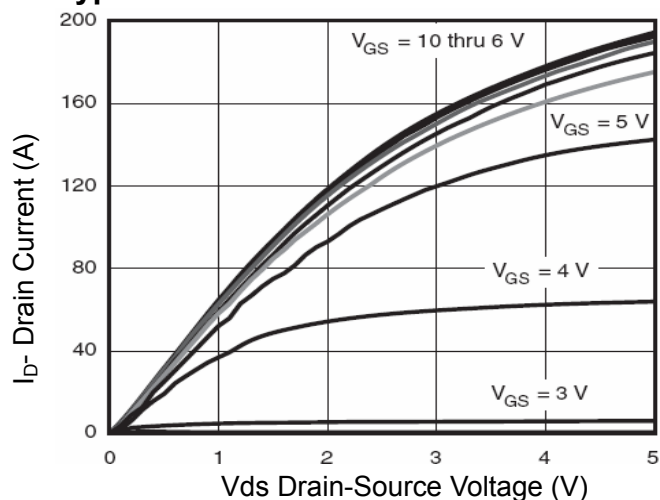


Figure 1 Output Characteristics

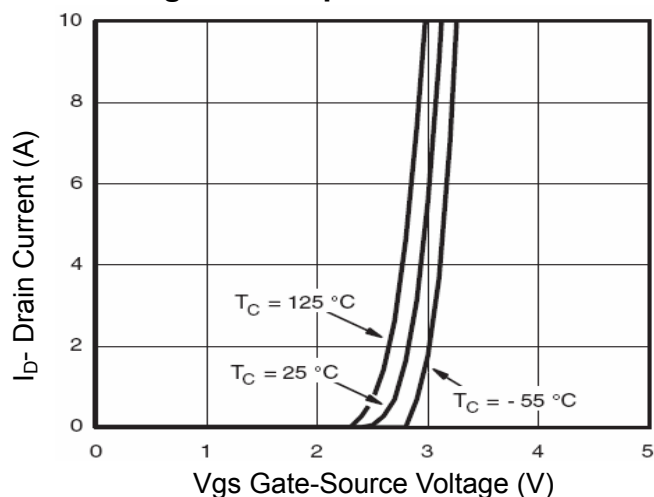


Figure 2 Transfer Characteristics

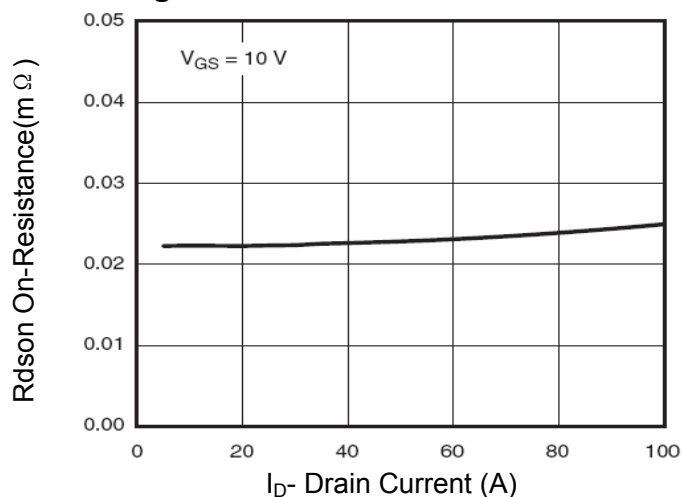


Figure 3 $R_{DS(on)}$ - Drain Current

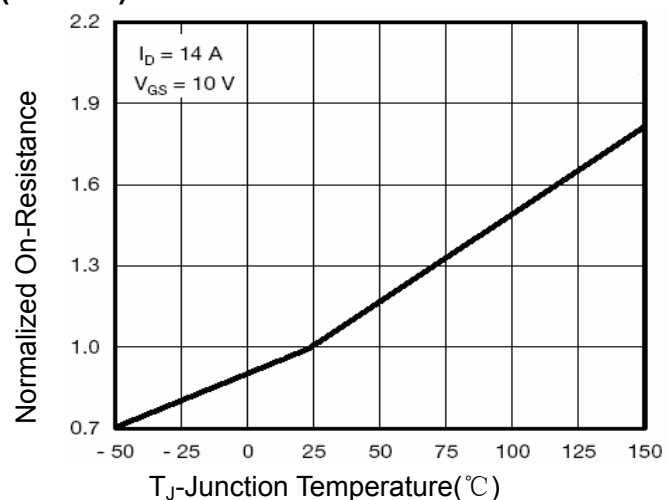


Figure 4 $R_{DS(on)}$ -Junction Temperature

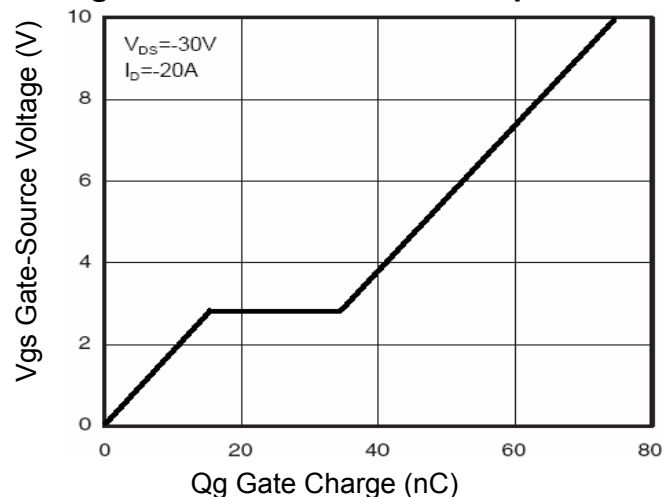


Figure 5 Gate Charge

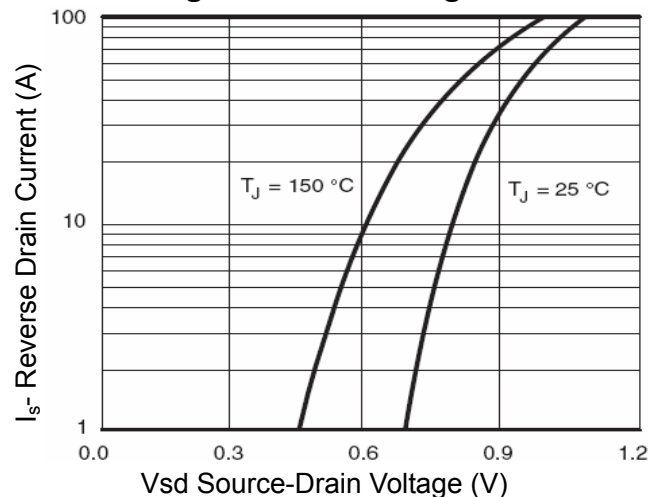


Figure 6 Source- Drain Diode Forward

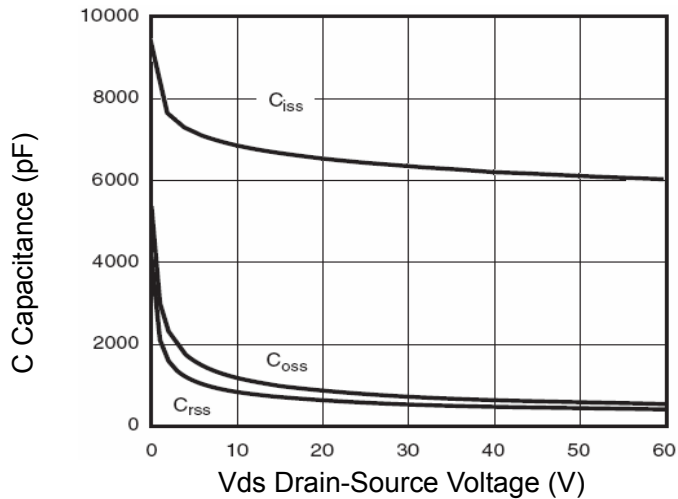


Figure 7 Capacitance vs Vds

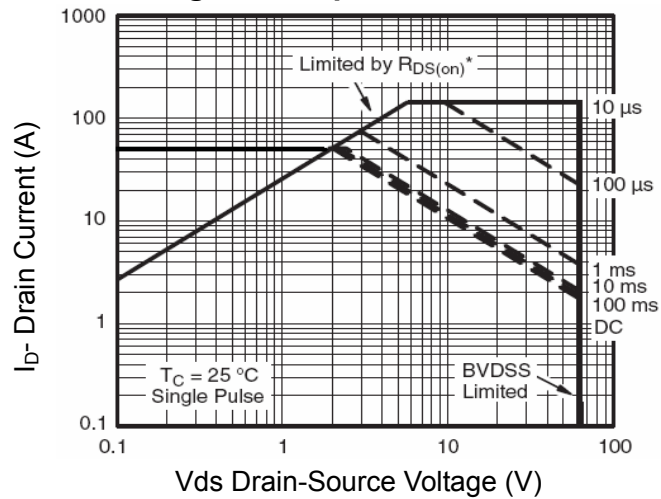


Figure 8 Safe Operation Area

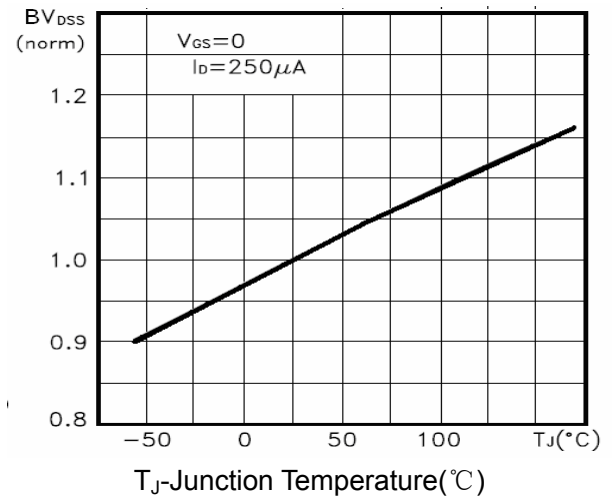


Figure 9 BV_{DSS} vs Junction Temperature

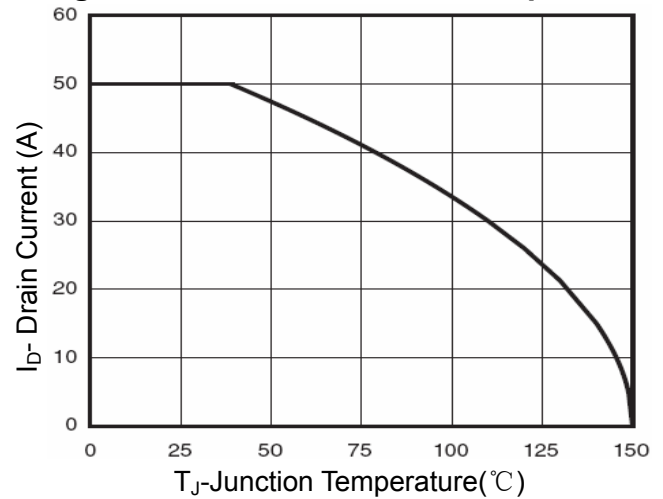


Figure 10 ID Current Derating vs Junction Temperature

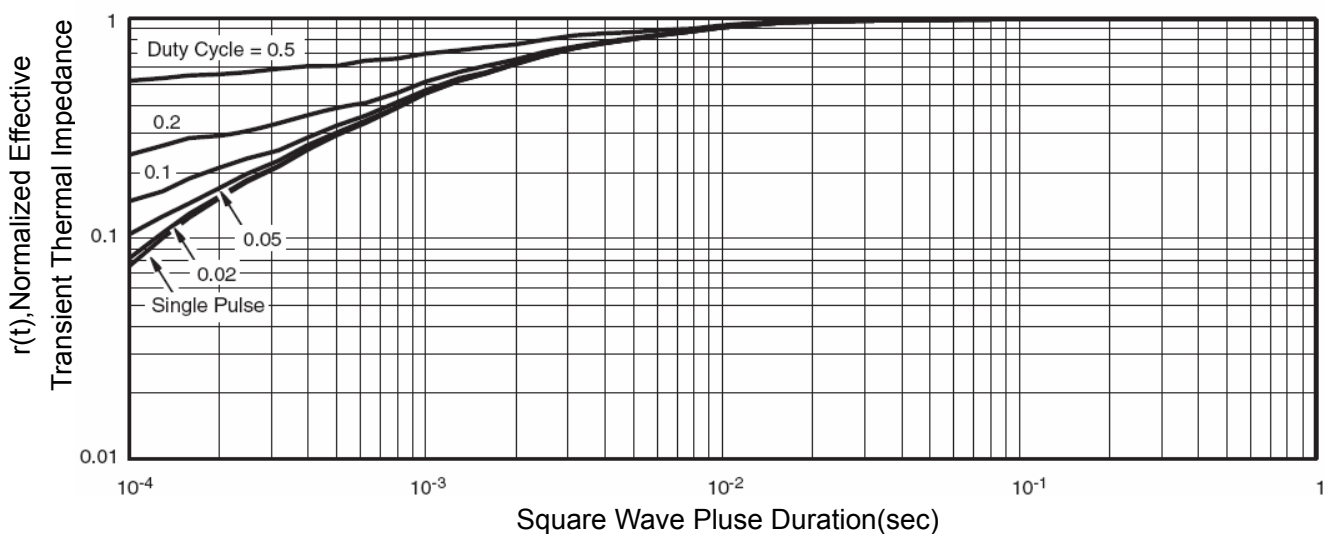
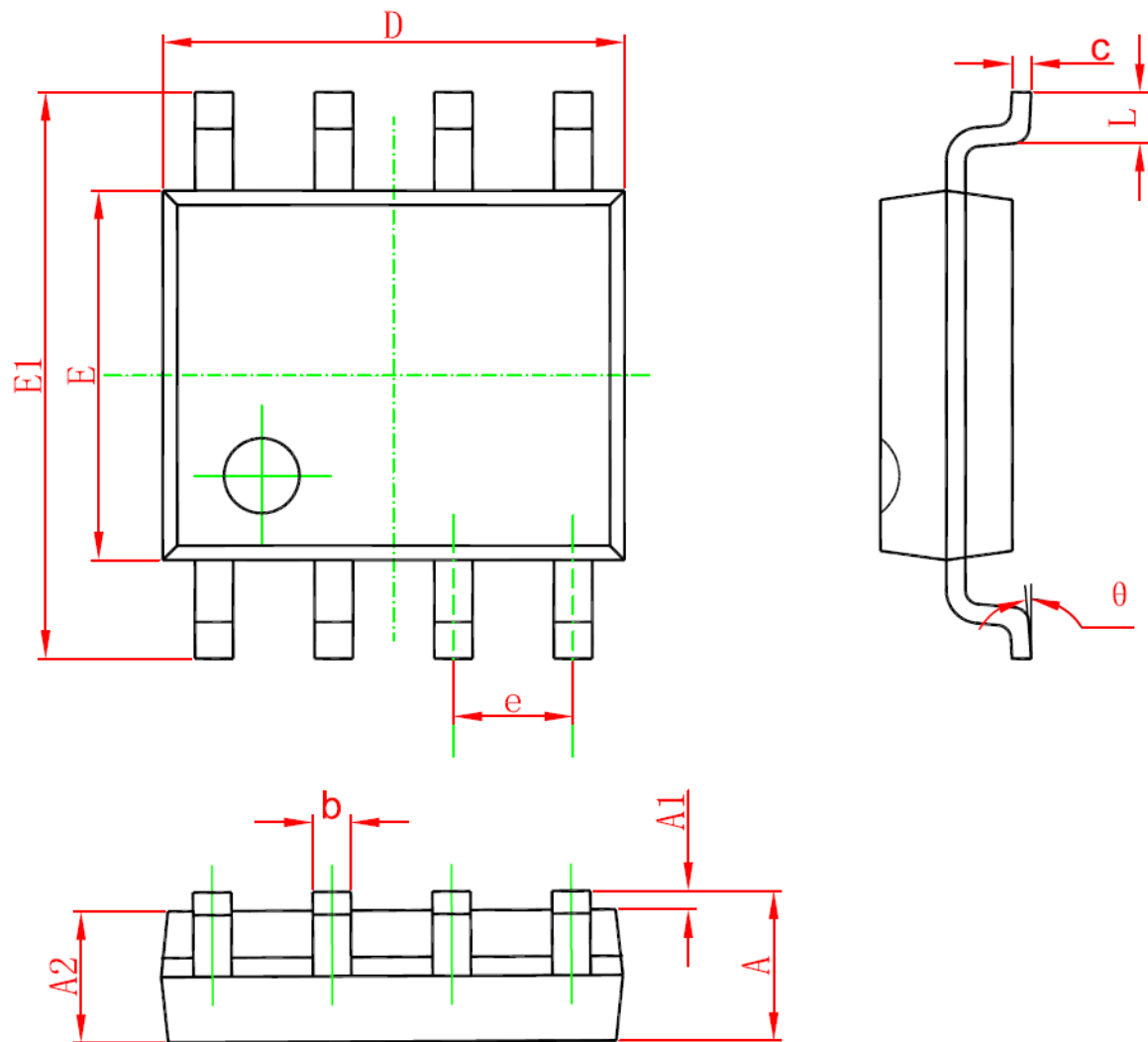


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°