

Description

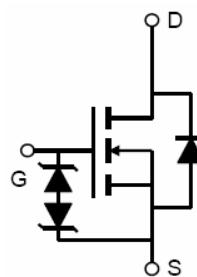
The HM4402CE uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

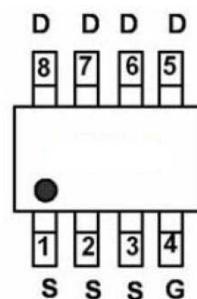
- $V_{DS} = 20V, I_D = 1GA$
- $R_{DS(ON)} < 1m\Omega @ V_{GS} = 4.5V$
- $R_{DS(ON)} < 1m\Omega @ V_{GS} = 2.5V$
- ESD Rating: 2000V HBM
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

Application

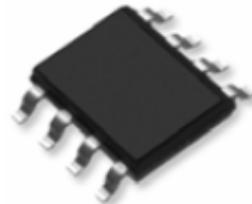
- PWM application
- Load switch



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4402CE	HM4402CE	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	1G	A
Pulsed Drain Current	I_{DM}	10	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	42	°C/W
---	-----------------	----	------

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

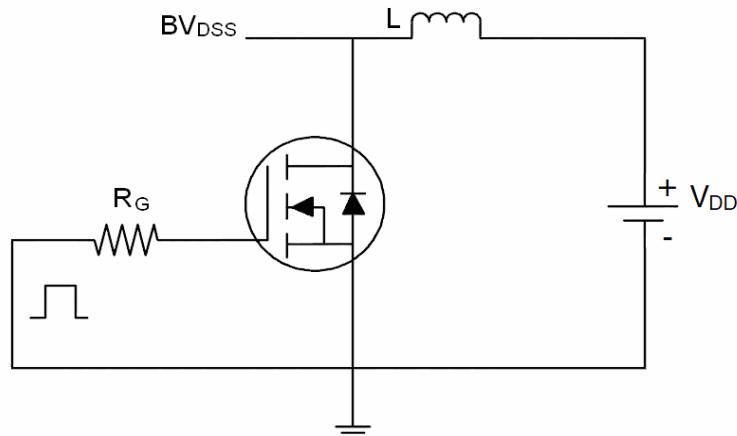
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	22	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 10\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 10	μA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.5	0.75	1.3	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=10\text{A}$	-	$\hat{\text{I}} \text{ H}$	$\hat{\text{I}} \text{ E}$	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=5.5\text{A}$	-	$\hat{\text{I}} \text{ H}$	11.5	
Forward Transconductance	g_{FS}	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=10\text{A}$	30	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C_{iss}	$V_{\text{DS}}=10\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	1710	-	PF
Output Capacitance	C_{oss}		-	232	-	PF
Reverse Transfer Capacitance	C_{rss}		-	200	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=10\text{V}, R_{\text{L}}=1\Omega$ $V_{\text{GS}}=10\text{V}, R_{\text{GEN}}=3\Omega$	-	2.5	-	nS
Turn-on Rise Time	t_r		-	7.2	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	49	-	nS
Turn-Off Fall Time	t_f		-	10.8	-	nS
Total Gate Charge	Q_g	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=10\text{A}, V_{\text{GS}}=4.5\text{V}$	-	17.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain Charge	Q_{gd}		-	4.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{s}}=10\text{A}$	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I_{s}		-	-	12	A

Notes:

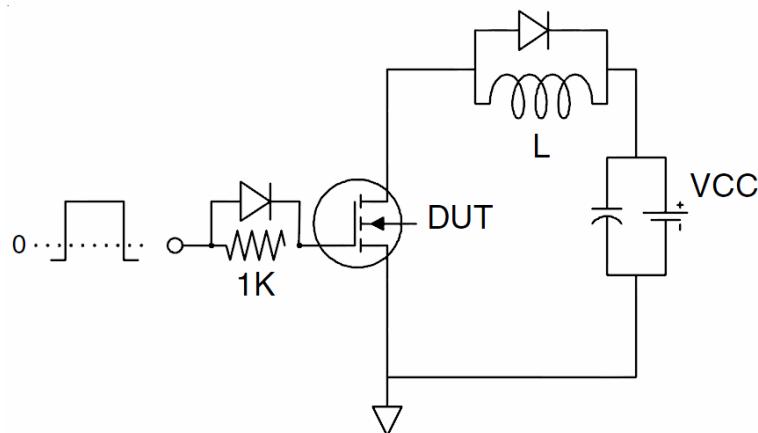
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

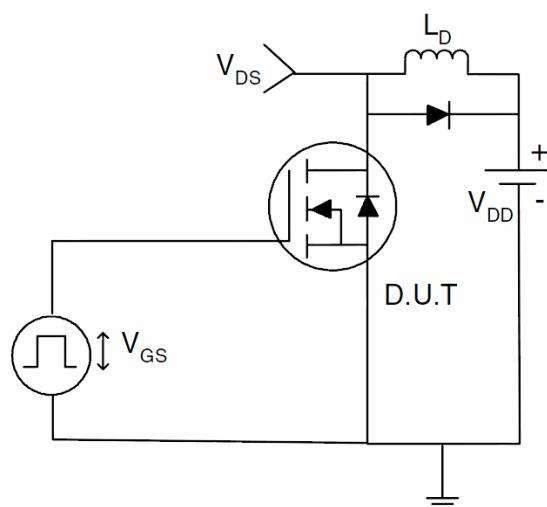
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

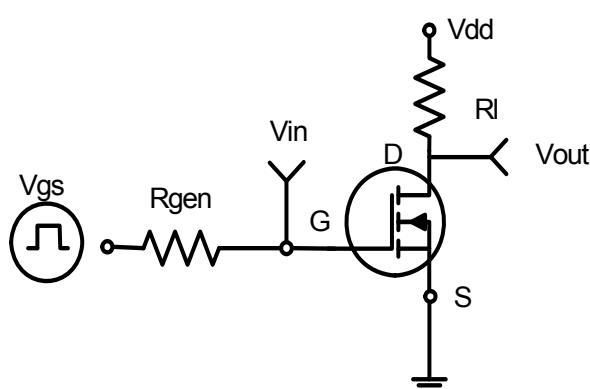


Figure 1:Switching Test Circuit

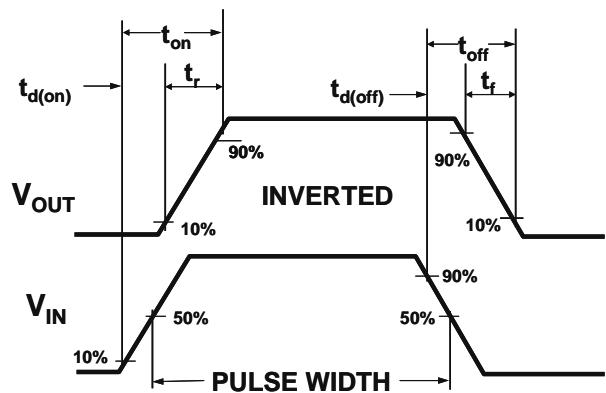


Figure 2:Switching Waveforms

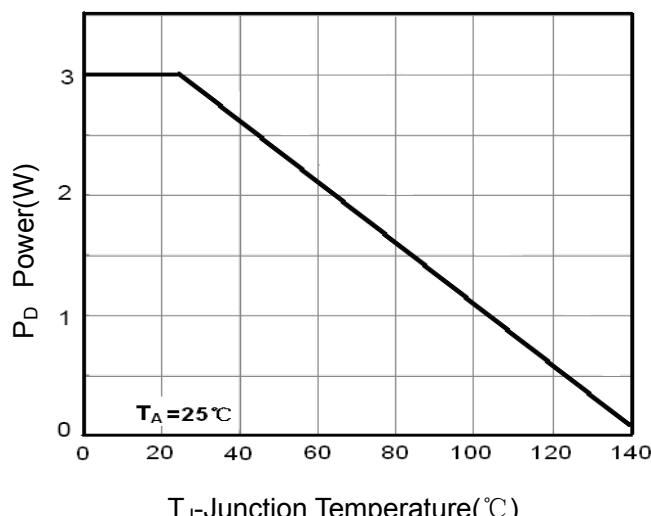


Figure 3 Power Dissipation

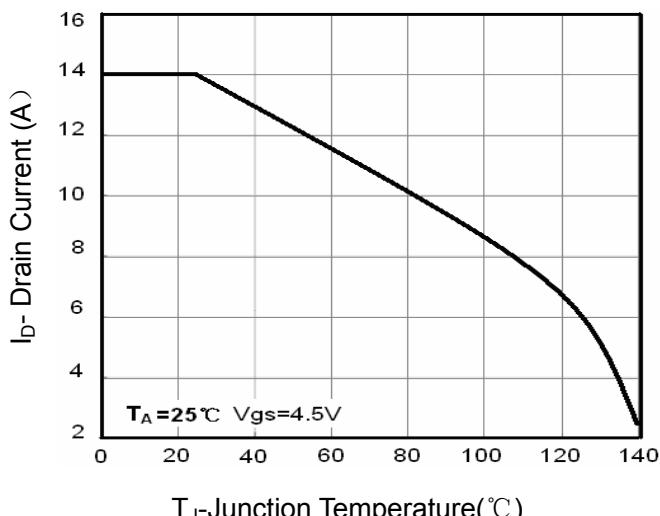


Figure 4 Drain Current

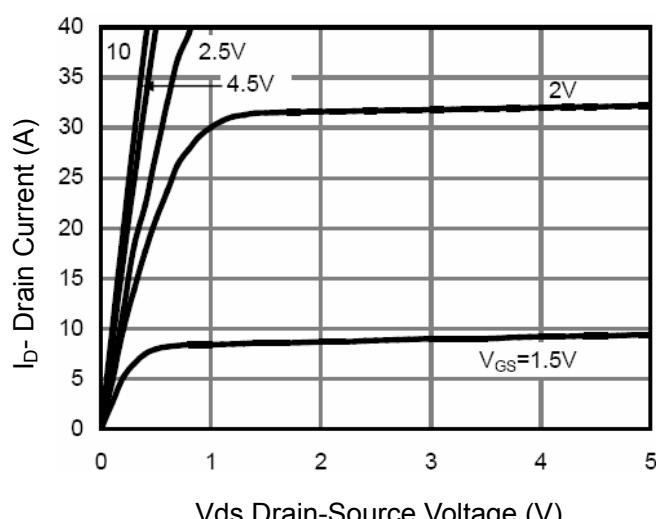


Figure 5 Output Characteristics

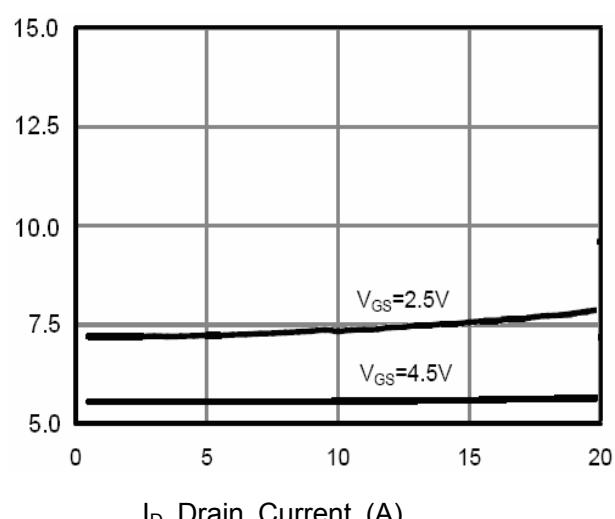


Figure 6 Drain-Source On-Resistance

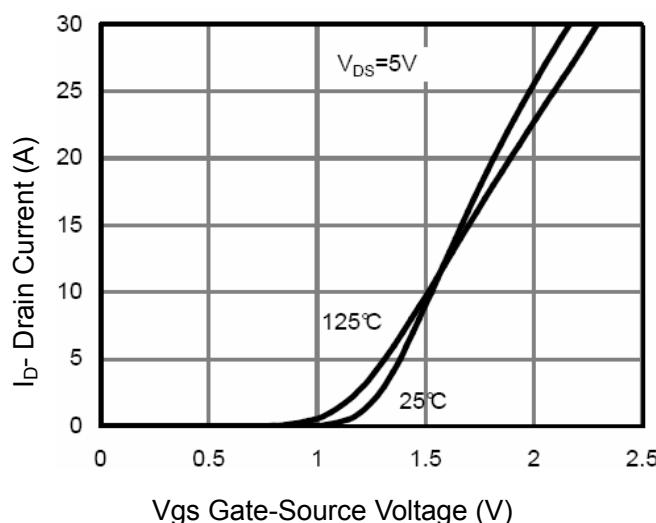


Figure 7 Transfer Characteristics

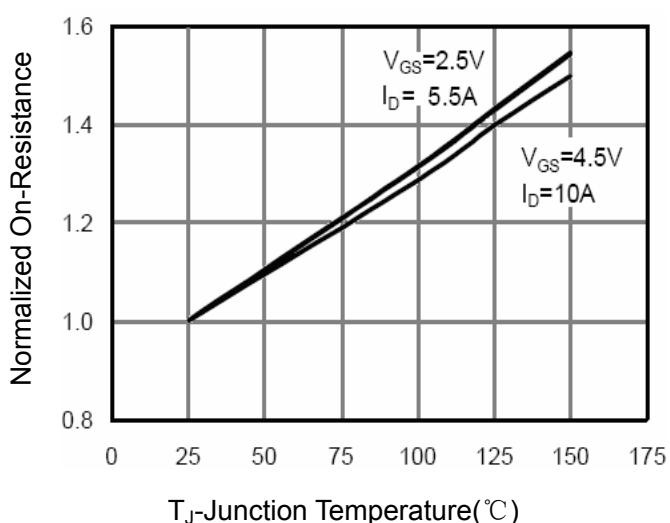


Figure 8 Drain-Source On-Resistance

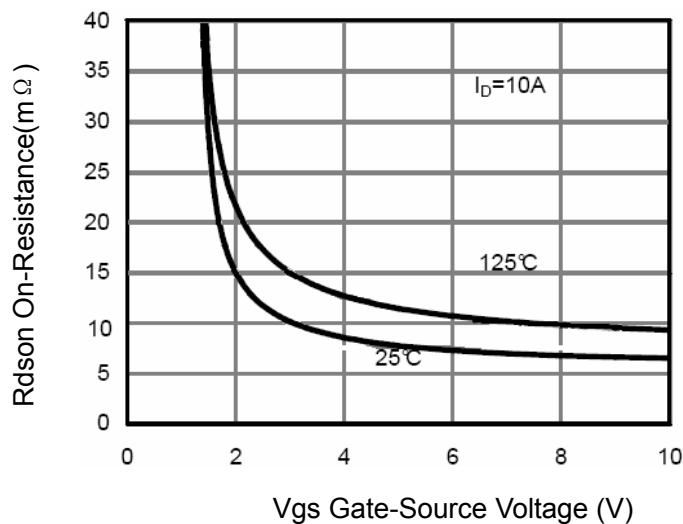


Figure 9 $R_{DS(on)}$ vs V_{GS}

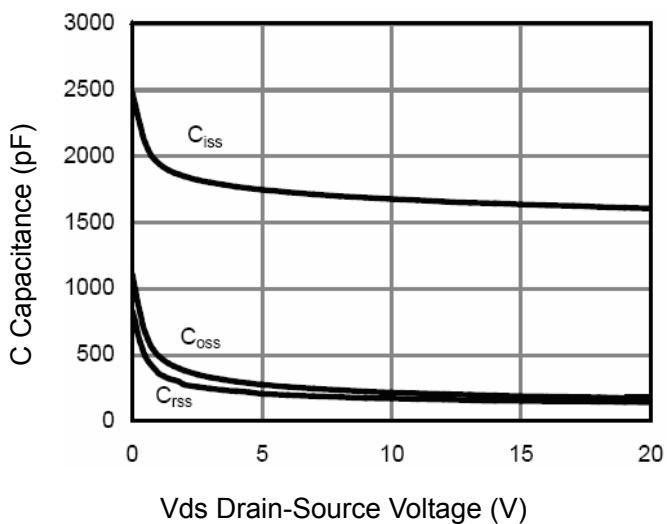


Figure 10 Capacitance vs V_{DS}

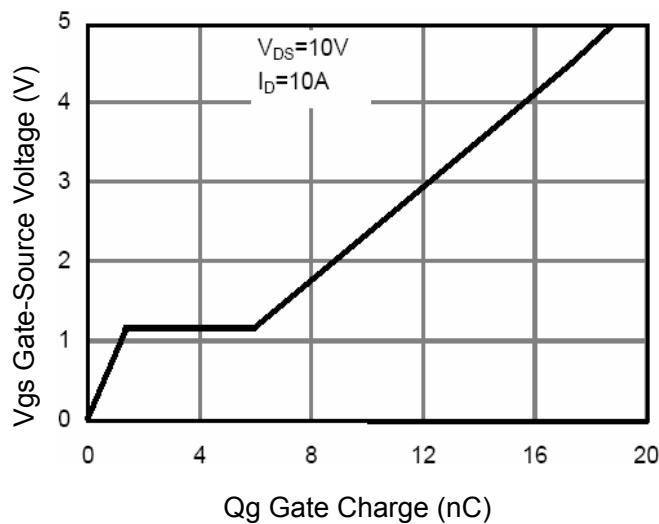


Figure 11 Gate Charge

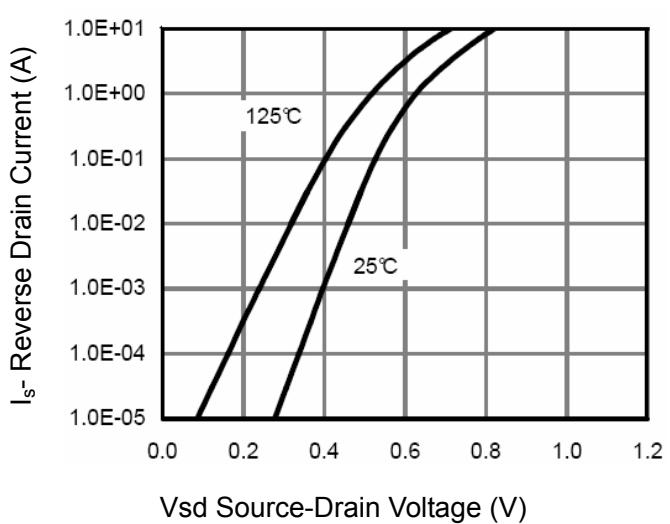


Figure 12 Source- Drain Diode Forward

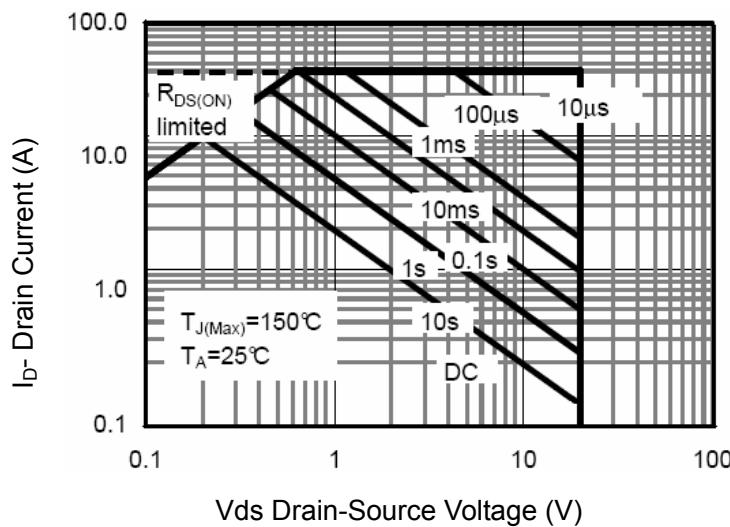


Figure 13 Safe Operation Area

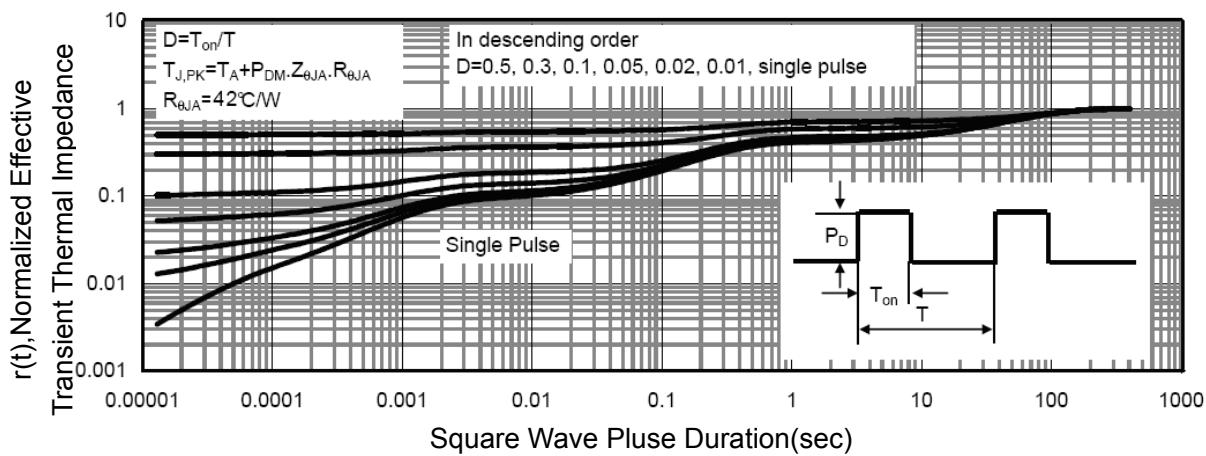
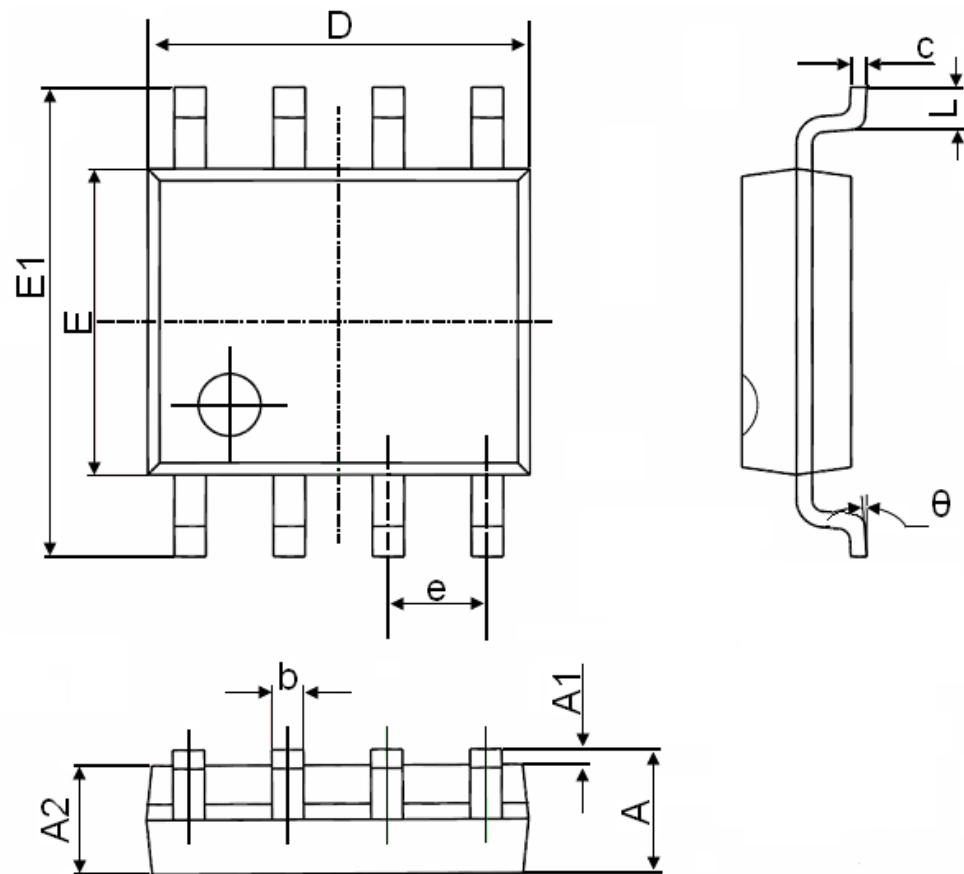


Figure 14 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°