

General Description:

HM3N150A the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-3P(H), which accords with the RoHS standard.

Features:

- Fast Switching
- Low ON Resistance($R_{ds(on)} \leq 8.0 \Omega$)
- Low Gate Charge (Typical Data: 9.3nC)
- Low Reverse transfer capacitances(Typical:2.4 pF)
- 100% Single Pulse avalanche energy Test

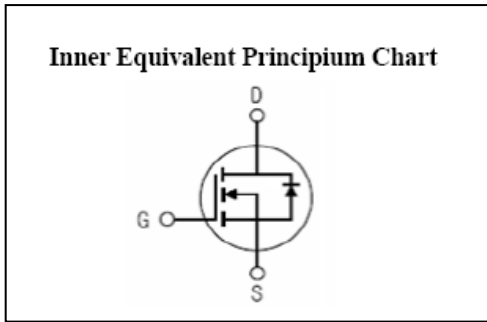
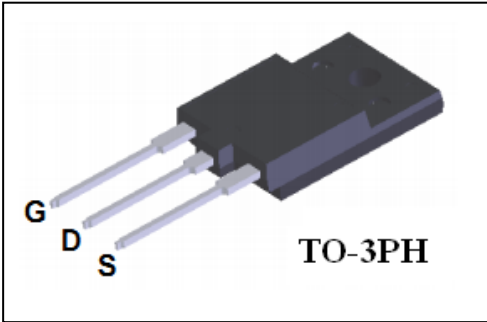
Applications:

Power switch circuit of adaptor and charger.

Absolute ($T_J = 25^{\circ}\text{C}$ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	1500	V
I_D	Continuous Drain Current $T_C = 25^{\circ}\text{C}$	3	A
	Continuous Drain Current $T_C = 100^{\circ}\text{C}$	1.8	A
I_{DM}^{a1}	Pulsed Drain Current $T_C = 25^{\circ}\text{C}$	12	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	227	mJ
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation $T_C = 25^{\circ}\text{C}$	TBD	W
	Derating Factor above 25°C	TBD	W/ $^{\circ}\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}\text{C}$
T_L	Maximum Temperature for Soldering	300	$^{\circ}\text{C}$

V_{DSS}	1500	V
I_D	3	A
$P_D(T_C=25^{\circ}\text{C})$	TBD	W
$R_{DS(ON)Typ}$	5.0	Ω



Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Unit
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	1500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A, \text{Reference } 25^\circ\text{C}$	--	1.3	--	V/ $^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=1500V, V_{GS}=0V, T_J=25^\circ\text{C}$	--	--	25	μA
		$V_{DS}=1200V, V_{GS}=0V, T_J=125^\circ\text{C}$	--	--	500	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=1.5A$	--	5.0	8.0	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	3.0	--	5.0	V
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Trans conductance	$V_{DS}=30V, I_D=1.5A$	--	4.5	--	S
R_g	Gate resistance	$f=1.0\text{MHz}$	--	3.5	--	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=25V, f=1.0\text{MHz}$	--	1938	--	pF
C_{oss}	Output Capacitance		--	104	--	
C_{rss}	Reverse Transfer Capacitance		--	2.4	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=3A, V_{DD}=750V, R_G=10\Omega$	--	33.8	--	ns
t_r	Rise Time		--	16.7	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	56.0	--	
t_f	Fall Time		--	27.6	--	
Q_g	Total Gate Charge	$I_D=3A, V_{DD}=750V, V_{GS}=10V$	--	9.3	--	nC
Q_{gs}	Gate to Source Charge		--	14.9	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	5.3	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I _S	Continuous Source Current (Body Diode)	T _C = 25 °C	--	--	3	A
I _{SM}	Maximum Pulsed Current (Body Diode)		--	--	12	A
V _{SD}	Diode Forward Voltage	I _S =3.0A, V _{GS} =0V	--	--	1.5	V
trr	Reverse Recovery Time	I _S =3.0A, T _J = 25 °C dI _F /dt=100A/us, V _{GS} =0V	--	302.3	--	ns
Qrr	Reverse Recovery Charge		--	9.9	--	nC
I _{RRM}	Reverse Recovery Current		--	1501.8	--	A
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	TBD	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	TBD	$^{\circ}\text{C}/\text{W}$

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10\text{mH}, I_D=6.7\text{A}, \text{Start } T_j=25\text{ }^{\circ}\text{C}$

^{a3}: $I_{SD}=3\text{A}, di/dt \leq 100\text{A}/\mu\text{s}, V_{DD} \leq BV_{DS}, \text{Start } T_j=25\text{ }^{\circ}\text{C}$

Test Circuit and Waveform:

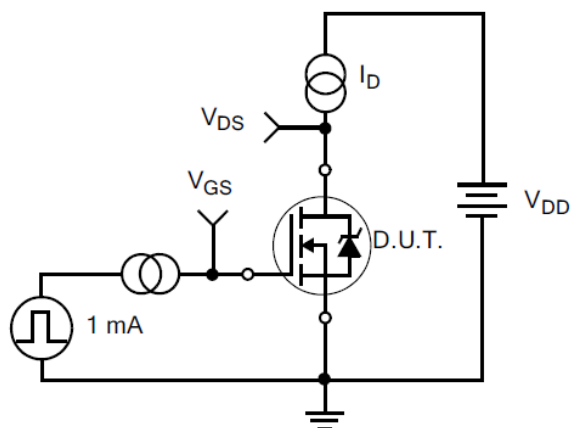


Figure 14. Gate Charge Test Circuit

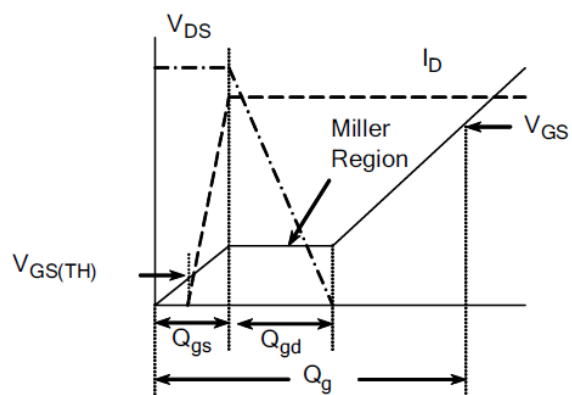


Figure 15. Gate Charge Waveforms

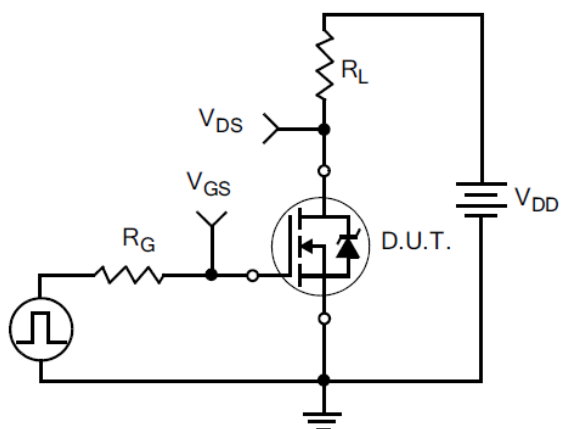


Figure 16. Resistive Switching Test Circuit

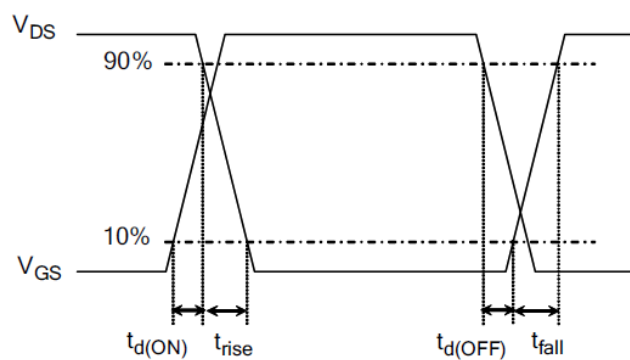


Figure 17. Resistive Switching Waveforms

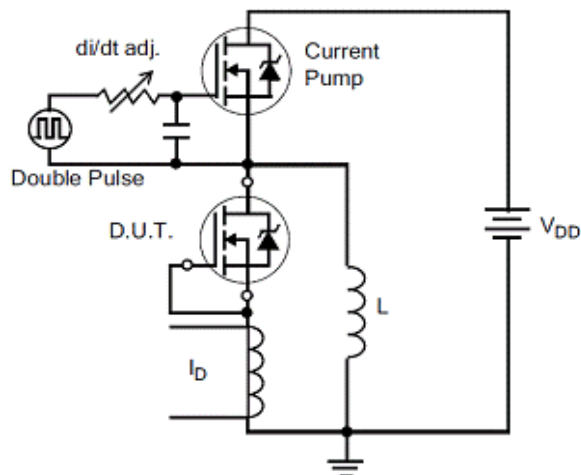


Figure 18. Diode Reverse Recovery Test Circuit

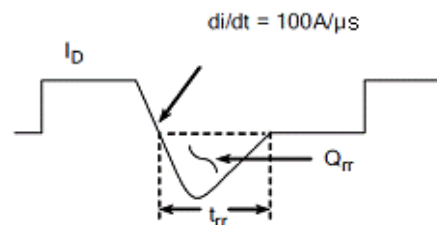


Figure 19. Diode Reverse Recovery Waveform

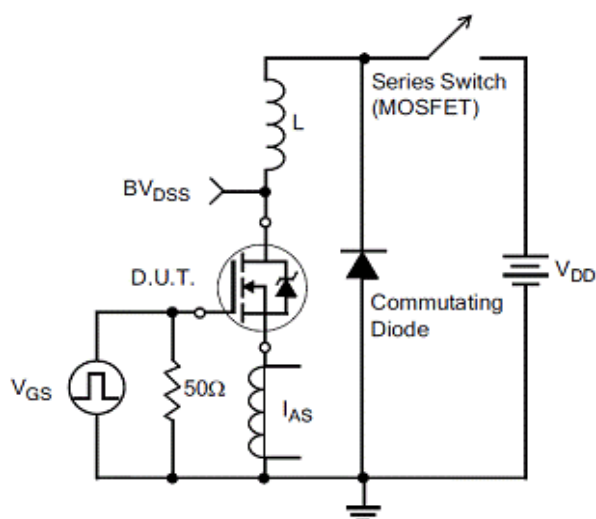


Figure20.Unclamped Inductive Switching Test Circuit

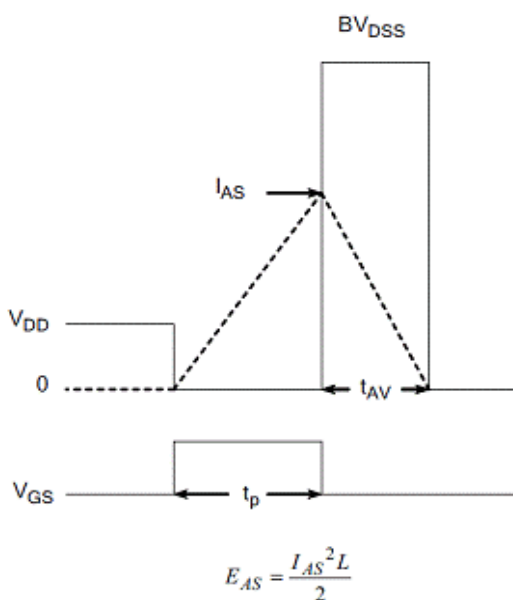
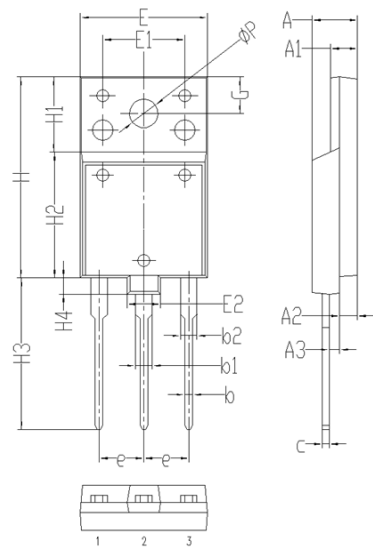


Figure21.Unclamped Inductive Switching Waveform

Package Information:



Items	Values(mm)	
	MIN	MAX
A	5.25	5.85
A1	2.7	3.3
A2	1.8	2.4
A3	1.0	1.6
b	0.45	1.05
b1	1.7	2.3
b2	1.7	2.3
c	0.6	1.2
e	5.15	5.75
E	15.2	15.8
E1	9.7	10.3
E2	3.7	4.3
H	24.2	24.8
H1	8.9	9.5
H2	15.0	15.6
H3	17.9	19.1
H4	1.7	2.3
H5	4.7	5.3
G	4.2	4.8
ΦP	3.3	3.9

TO-3P(H) Package