HM30P03Q

-30V_{DS}／±20V_{GS}／-30A(I_D) P-Channel Enha ncement Mode MOSFET

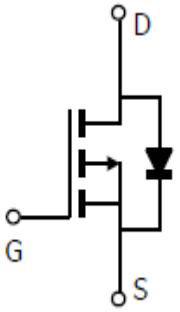
Features

- V_{DSS}=-30V／V_{GSS}=±20V／I_D=-30A
  $R_{DS(ON)}$=14mΩ(max.)@V_{GS}=-10V
  $R_{DS(ON)}$=22mΩ(max.)@V_{GS}=-4.5V
- Low Dense Cell Design
- Reliable and Rugged
- Advanced trench process technology

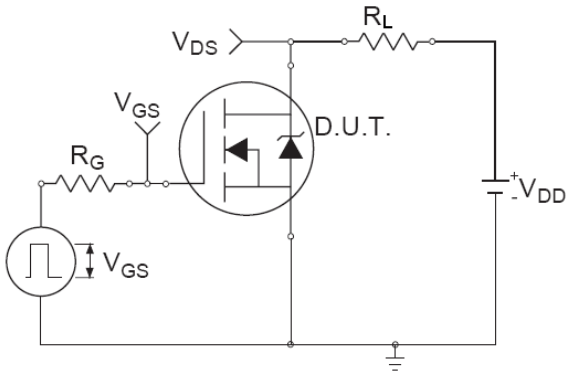
Applications

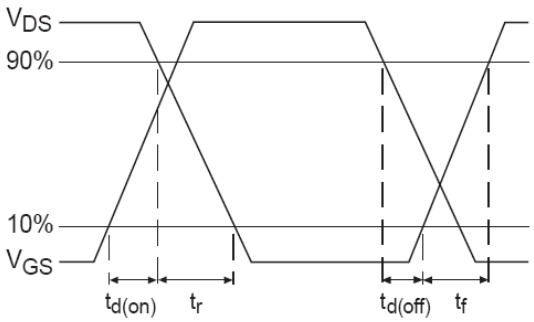
- Synchronous Rectification
- Power Management in Inverter System

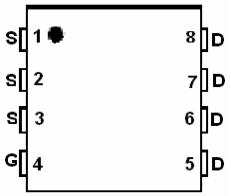
Pin Description



Marking and pin Assignment







Marking and pin assignment

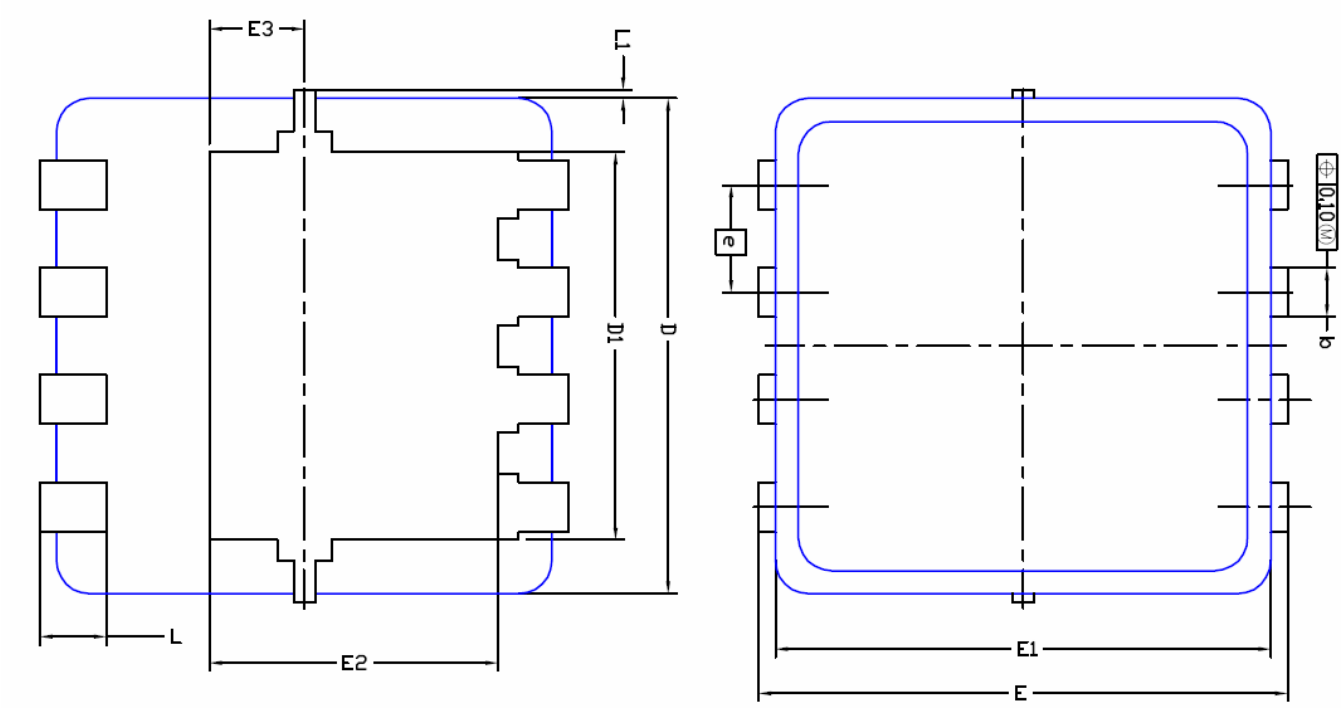
Package Marking and Ordering Information

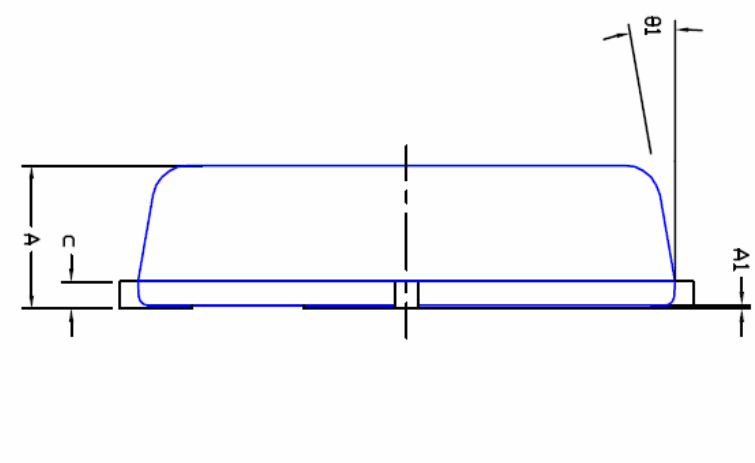
Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM30P03Q	HM30P03Q	DFN3X3-8L	-	-	-

Electrical Characteristics of CP Test (TA=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=-250uA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V,V_{GS}=0V			1	uA
		T_J=85°C			30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250uA	-1	-1.65	-3	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V			±100	nA
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-30A			14	mΩ
		V_{GS}=-4.5V, I_D=-21A			22	
V_{SD}	Diode Forward Voltage	I_{SD}=-8A,V_{GS}=0V			-1.3	V
R_G	Gate Resistance	V_{GS}=0V, V_{DS}=0V, Frequency=1MHz		6		Ω

Note: 1: Pulse test ; pulse width ≦ 300ns, duty cycle ≦ 2%.
2: Guaranteed by design, not subject to production testing.





DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°