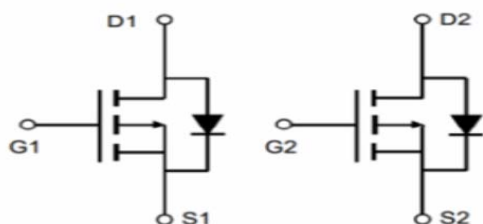
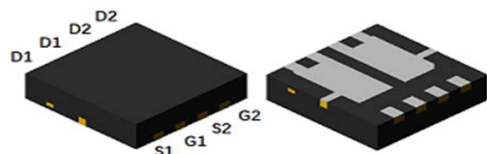


P-Channel Enhancement Mode Field Effect Transistor

DFN3.3X3.3



Product Summary

- V_{DS} -20V
- I_D -18A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) <32mohm
- $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) <40mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current ^B	$T_A=25^\circ\text{C}$ @ Steady State	I_D	-18	A
	$T_A=100^\circ\text{C}$ @ Steady State		-12.6	
Drain Current ^B	$T_A=25^\circ\text{C}$ @ Steady State	I_D	-18	A
	$T_A=70^\circ\text{C}$ @ Steady State		-16.2	
Pulsed Drain Current ^A		I_{DM}	-55	A
Single Pulse Avalanche Energy ^B		E_{AS}	31	mJ
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$ @ Steady State	P_D	32	W
	$T_A=100^\circ\text{C}$ @ Steady State		12.8	
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$ @ Steady State	P_D	32	W
	$T_A=70^\circ\text{C}$ @ Steady State		12.8	
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JC}$	3.9	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case @ Steady State ^C		$R_{\theta JA}$	42	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
HM18DP03Q	F1	HM18DP03Q	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V,V _{GS} =0V,T _C =25℃			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.35		-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -2.5V, I _D =-2A			40	mΩ
		V _{GS} = -4.5V, I _D =-4A			32	
Diode Forward Voltage	V _{SD}	I _S =-18A,V _{GS} =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-18	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V,V _{GS} =0V,f=1MHZ		2992		pF
Output Capacitance	C _{oss}			330		
Reverse Transfer Capacitance	C _{rss}			272		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V,V _{DS} =-15V,I _D =-9.1A		72.8		nC
Gate Source Charge	Q _{gs}			6.6		
Gate Drain Charge	Q _{gd}			10.1		
Reverse Recovery Charge	Q _{rr}	I _F =-6A, di/dt=100A/us		34		
Reverse Recovery Time	t _{rr}			67		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V,V _{DS} =-15V, I _D =-6A, R _{GEN} =2.5Ω		7		ns
Turn-on Rise Time	t _r			33		
Turn-off Delay Time	t _{D(off)}			130		
Turn-off Fall Time	t _f			132		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

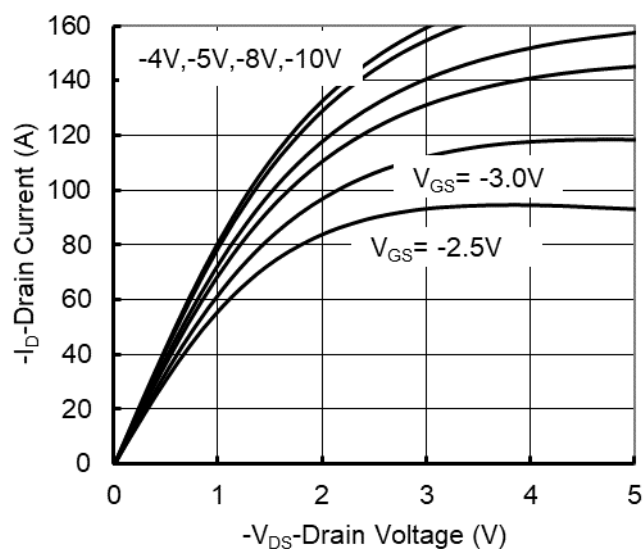


Figure 1. Output Characteristics

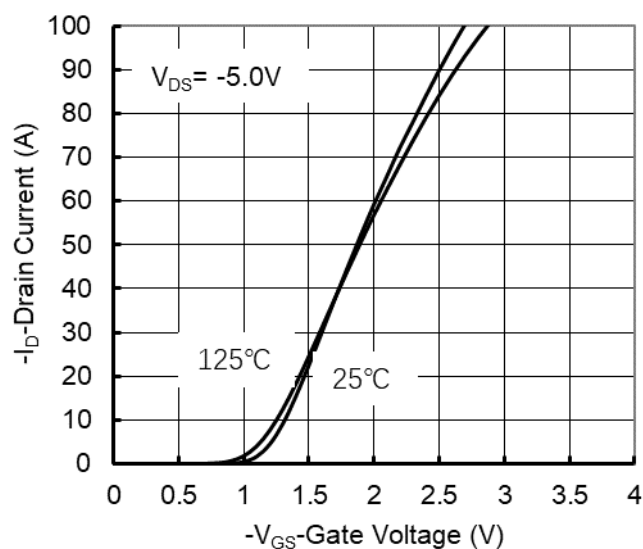


Figure 2. Transfer Characteristics

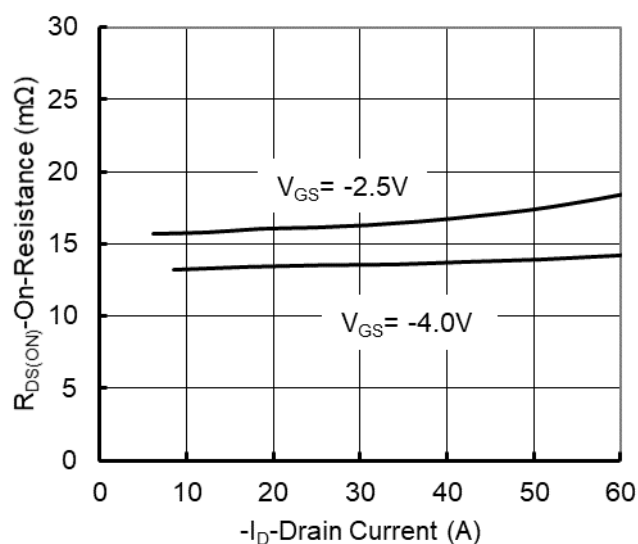


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

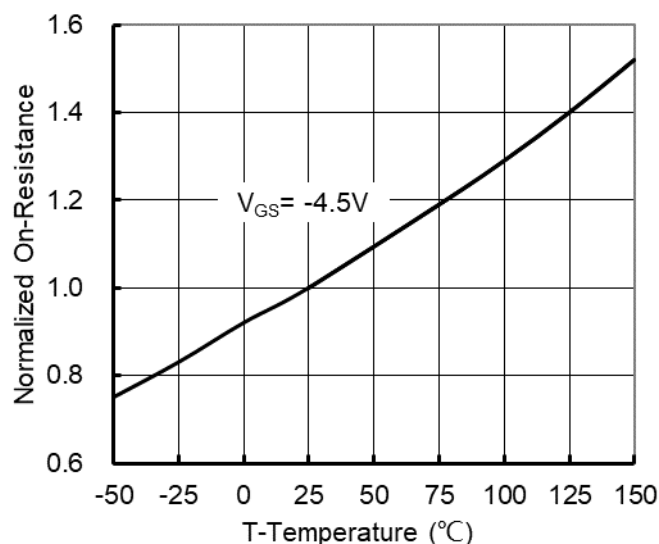


Figure 4. On-Resistance vs. Junction Temperature

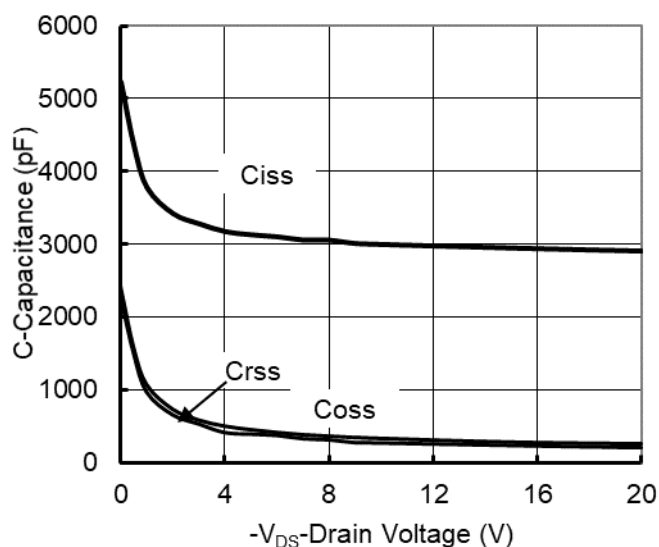


Figure 5. Capacitance Characteristics

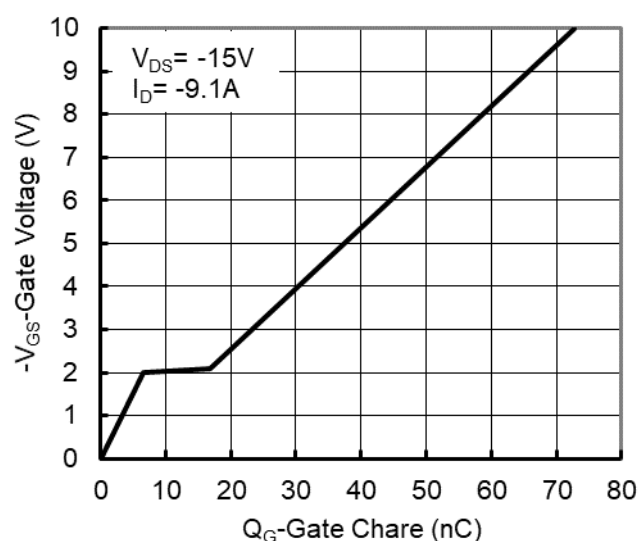


Figure 6. Gate Charge

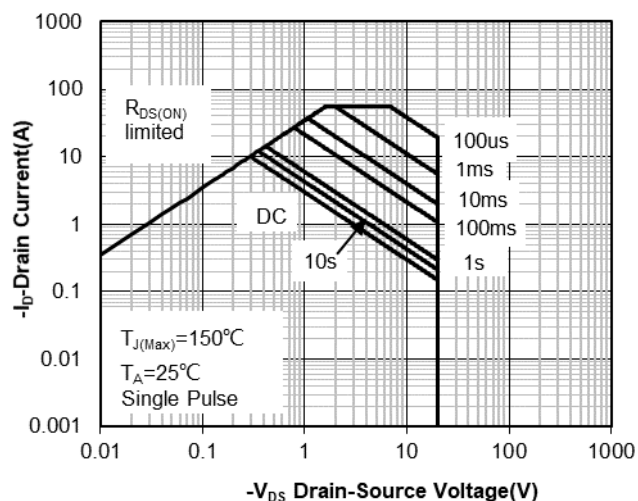


Figure 7. Safe Operation Area

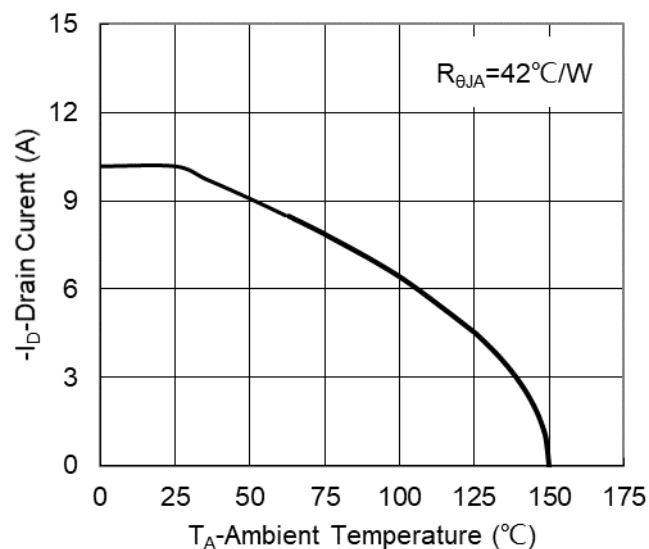


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

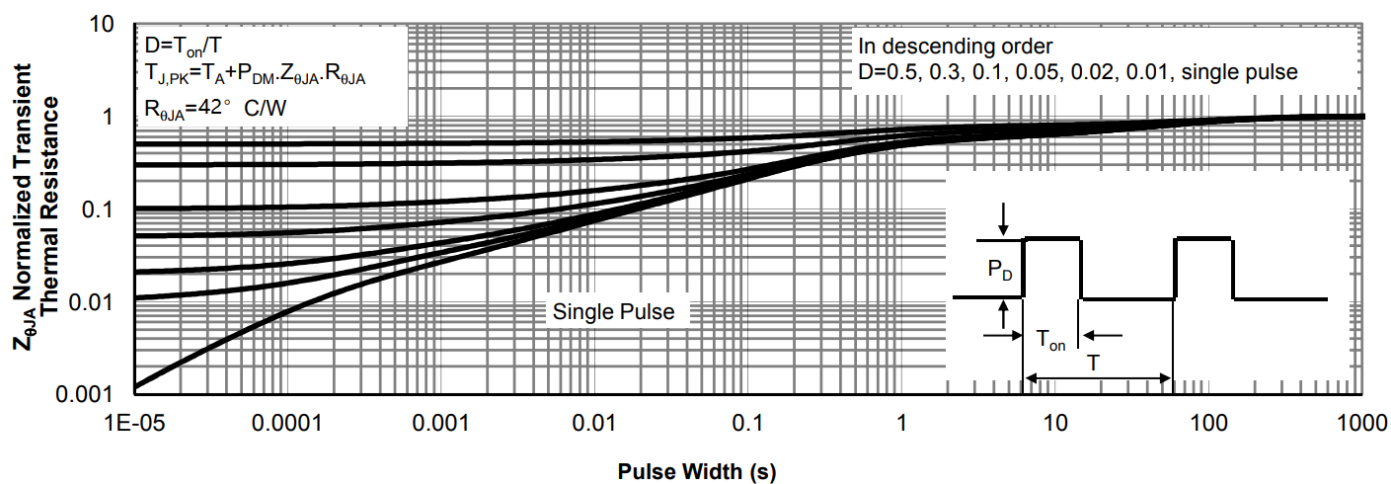
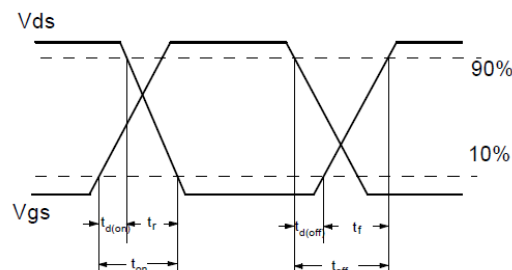
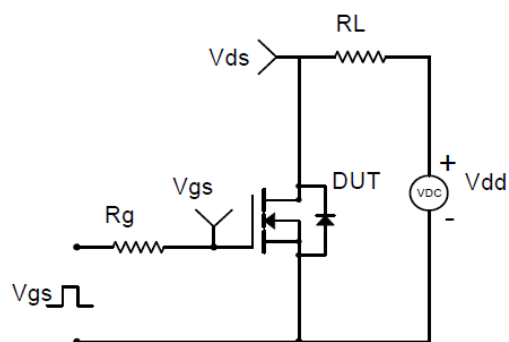
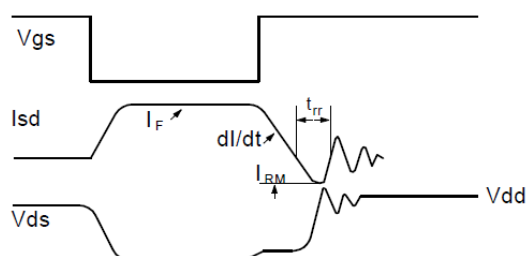
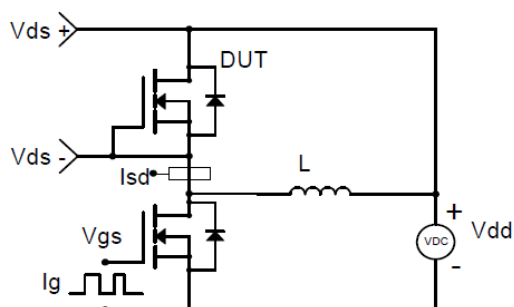


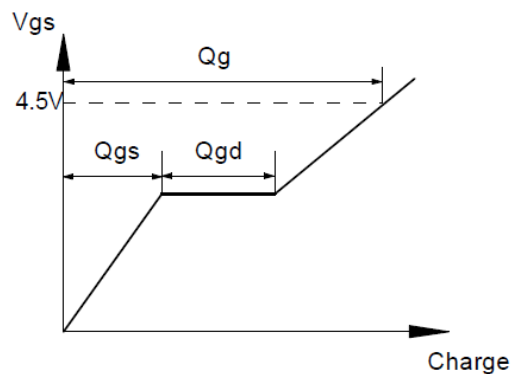
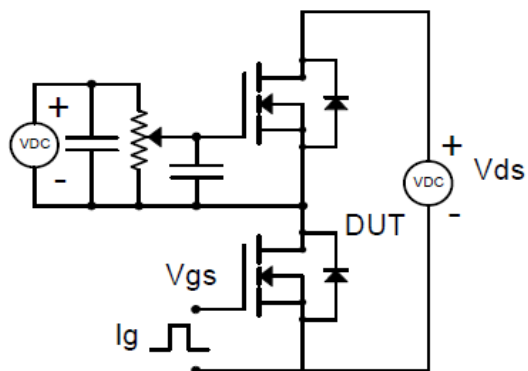
Figure 9. Normalized Maximum Transient Thermal Impedance



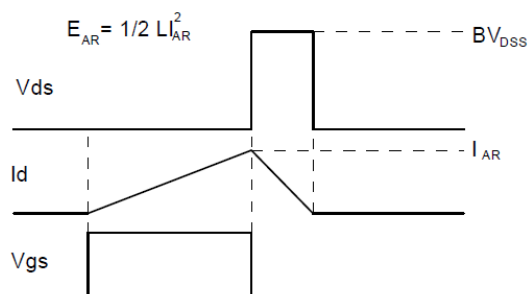
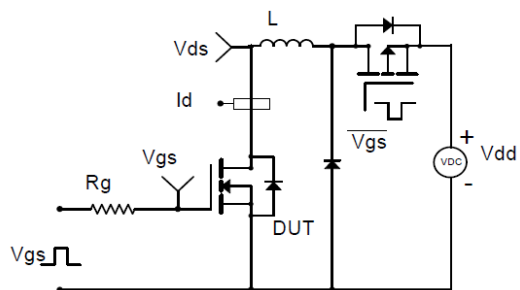
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

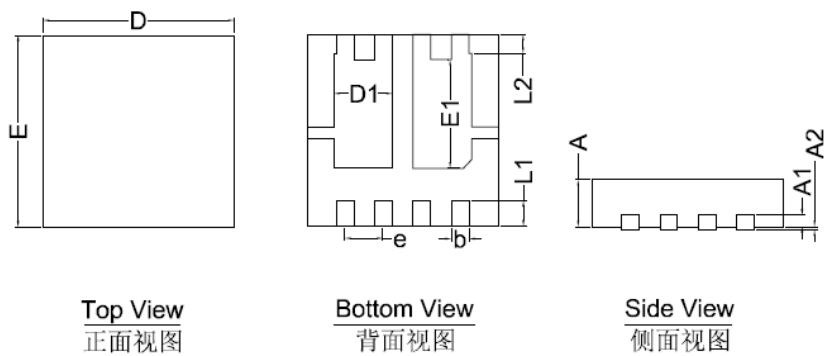


Gate Charge Test Circuit & Waveform

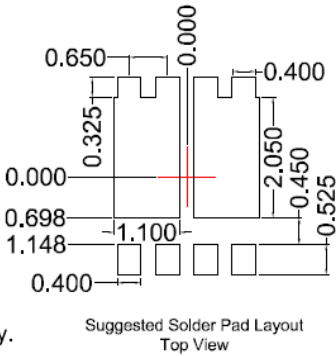


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■DFN3.3X3.3 Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
L1	0.325	0.425	0.525
L2	0.325 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Suggested Solder Pad Layout
Top View