

HM15N50/HM15N50F **500V N-Channel MOSFET**

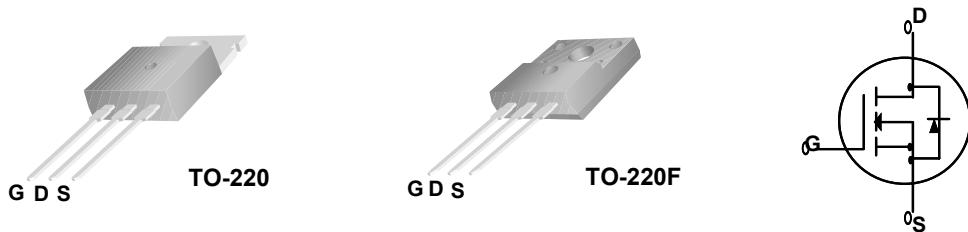
General Description

This Power MOSFET is produced using SL semi's advanced planar stripe DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 15.0A, 500V, $R_{DS(on)} = 0.42\Omega$ @ $V_{GS} = 10$ V
- Low gate charge (typical 45nC)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	HM15N50	HM15N50F	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	15.0	15.0*	A
	- Continuous ($T_C = 100^\circ\text{C}$)	8.0	8.0 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	52	*
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	860	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	19.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	195	48	W
	- Derate above 25°C	1.56	0.39	$\text{W}/^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	HM15N50	HM15N50F	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.64	2.58	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

Typical Characteristics

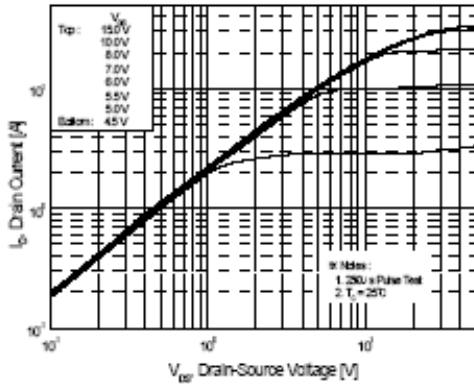


Figure 1. On-Region Characteristics

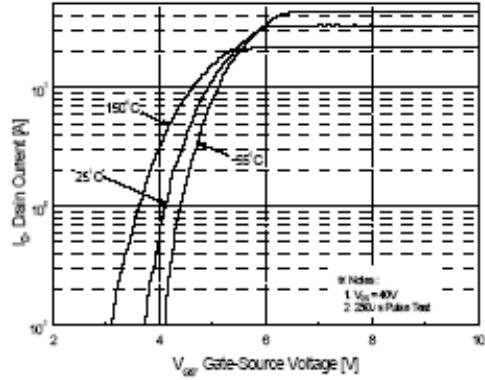


Figure 2. Transfer Characteristics

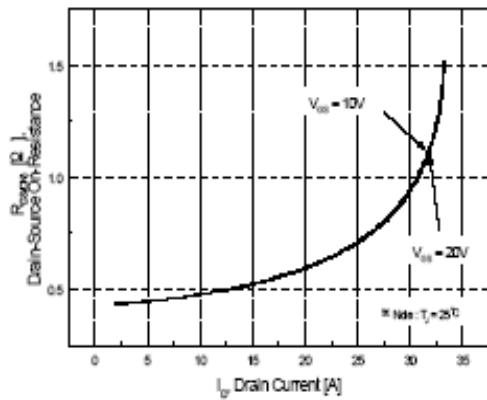


Figure 3. On-Resistance Variation vs
Drain Current and Gate Voltage

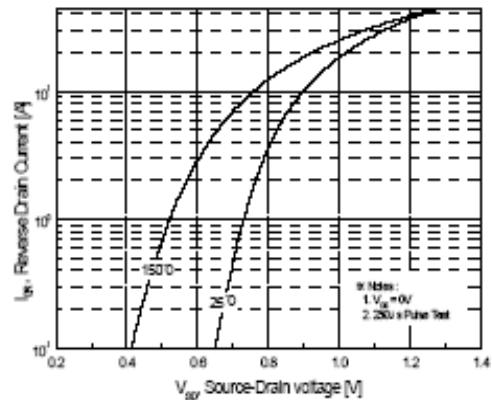


Figure 4. Body Diode Forward Voltage
Variation with Source Current

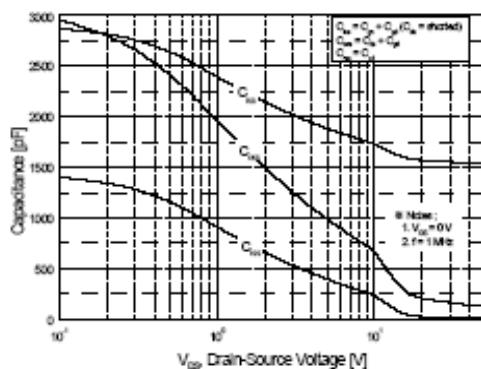


Figure 5. Capacitance Characteristics

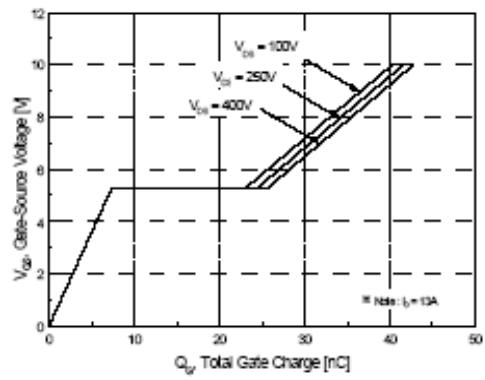
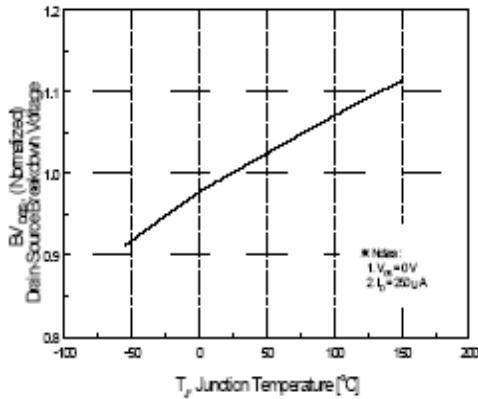
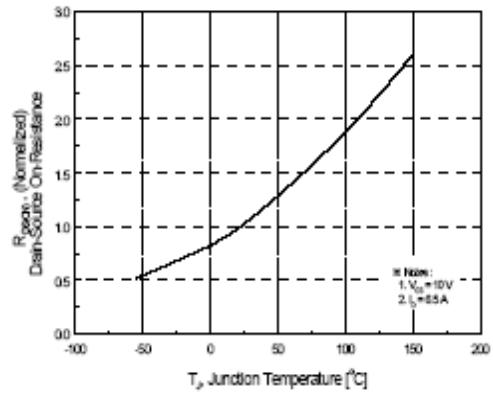


Figure 6. Gate Charge Characteristics

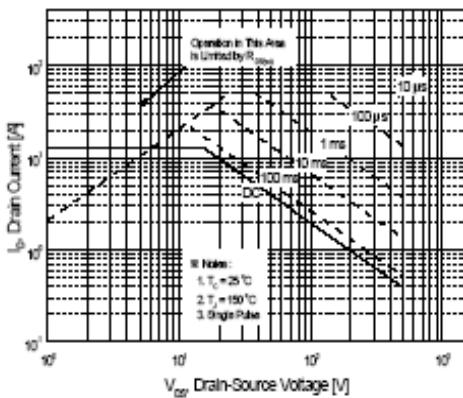
Typical Characteristics (Continued)



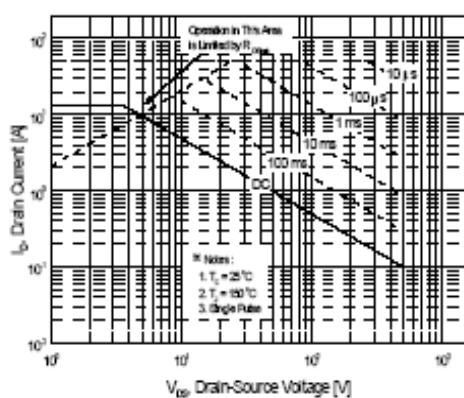
**Figure 7. Breakdown Voltage Variation
vs Temperature**



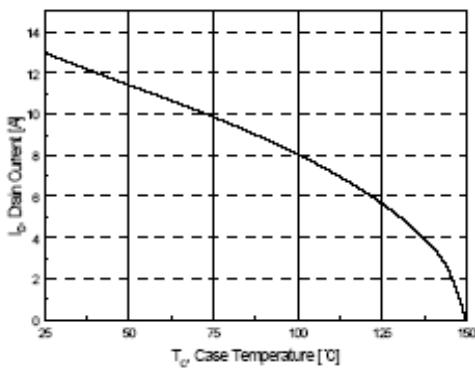
**Figure 8. On-Resistance Variation
vs Temperature**



**Figure 9-1. Maximum Safe Operating Area
for HM15N50**



**Figure 9-2. Maximum Safe Operating Area
for HM15N50F**



**Figure 10. Maximum Drain Current
vs Case Temperature**

Typical Characteristics (Continued)

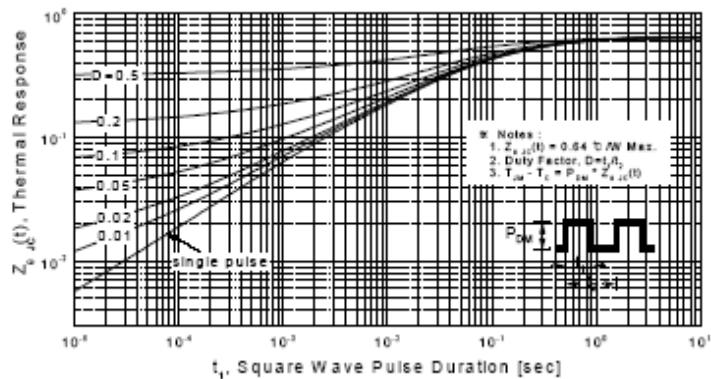


Figure 11-1. Transient Thermal Response Curve
for HM15N50

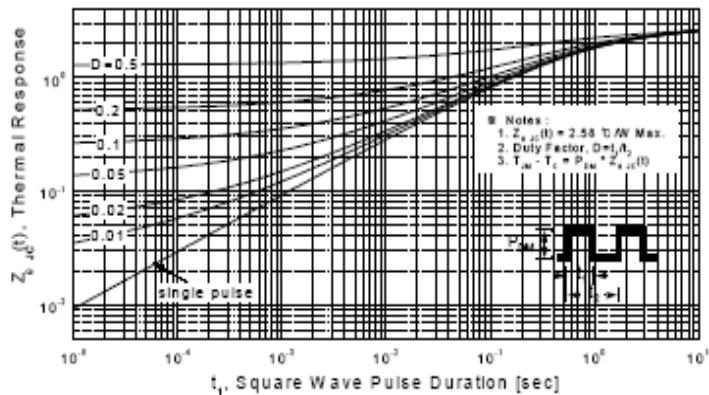
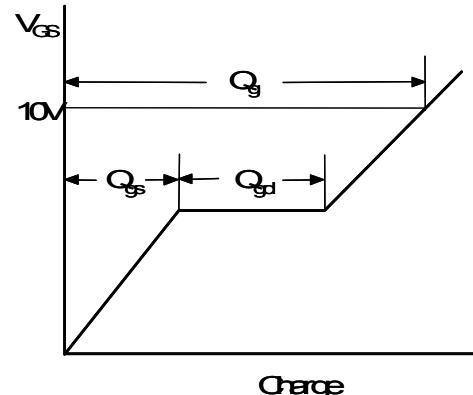
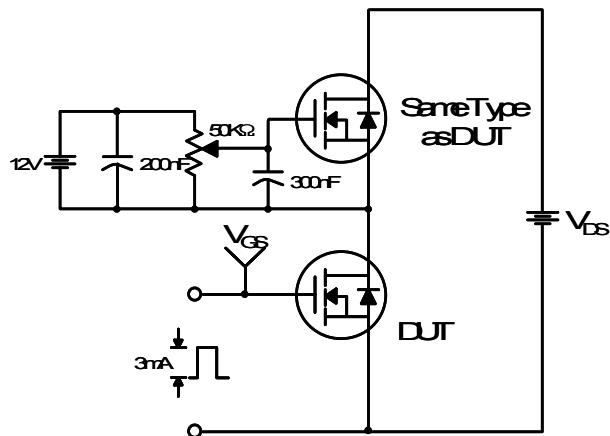
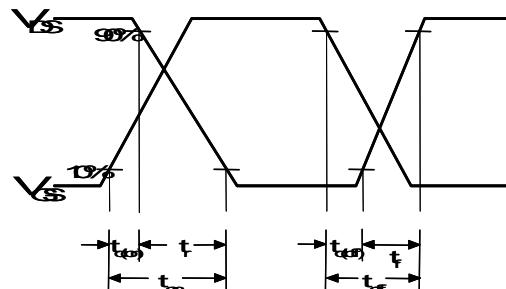
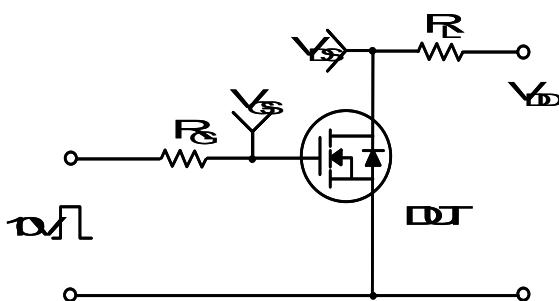


Figure 11-2. Transient Thermal Response Curve
for HM15N50F

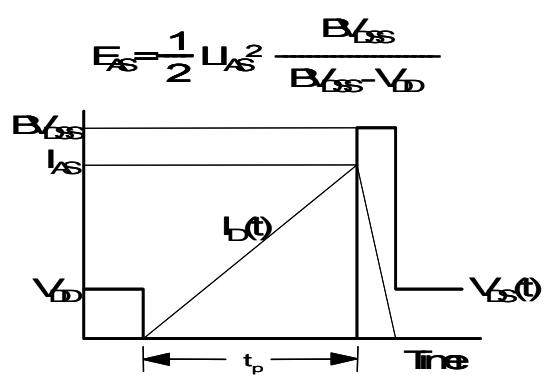
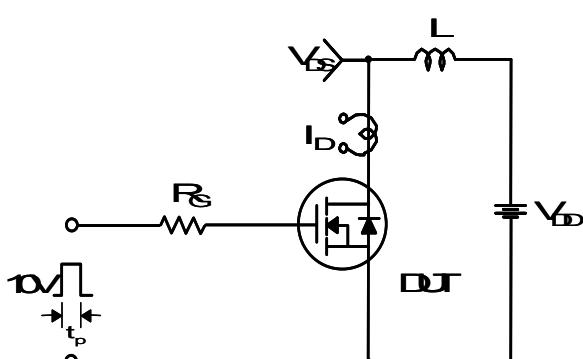
Gate Charge Test Circuit & Waveform



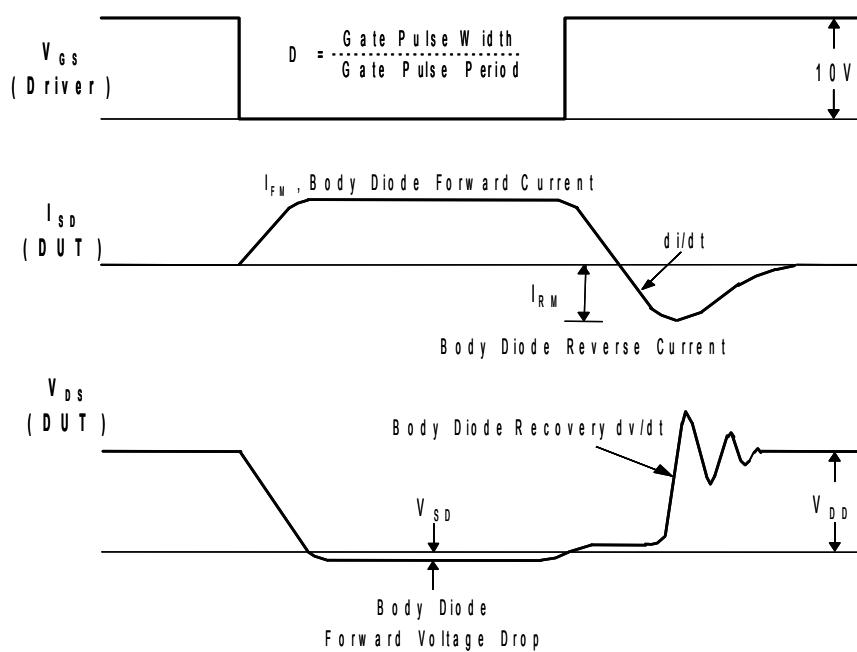
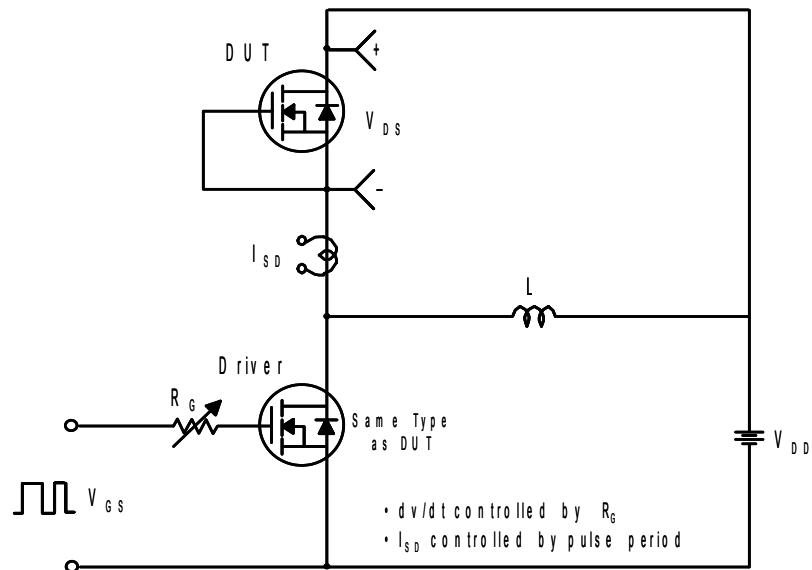
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



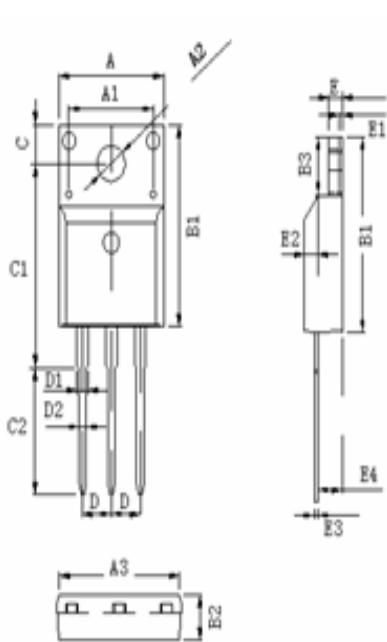
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220F

TO-220F 外形尺寸图



DIM.	MILLIMETERS
A	10.03 ± 0.20
A1	7.00
A2	3.12 ± 0.10
A3	9.70 ± 0.20
B1	15.75 ± 0.20
B2	4.72 ± 0.20
B3	6.70 ± 0.20
C	3.30 ± 0.10
C1	15.80 ± 0.20
C2	9.80 ± 0.2
D	Typical 2.54
D1	1.47 (MAX)
D2	0.80 ± 0.10
E	2.55 ± 0.20
E1	0.70
E2	1.00 × 45°
E3	0.50
E4	2.80 ± 0.20